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Doctoral thesis

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Development of radiation resistant CMOS integrated circuits for the power distribution system in the upgraded ATLAS Semiconductor Tracker

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Declaration of the author of this dissertation:

Aware of legal responsibility for making untrue statements I hereby declare that I have written this dissertation myself and all the contents of the dissertation have been obtained by legal means.

data, podpis autora

Declaration of the thesis Supervisor:

This dissertation is ready to be reviewed.

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Michał Bochenek
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Per me si va ne la città dolente,
per me si va ne l'etterno dolore,
per me si va tra la perduta gente.
Giustizia mosse il mio alto fattore;
fecemi la divina podestate,
la somma sapïenza e 'l primo amore.
Dinanzi a me non fuor cose create
se non etterne, e io etterno duro.
Lasciate ogne speranza, voi ch'intrate.

Dante Alighieri,
Divina Commedia

Streszczenie

Ogromny rozwój w dziedzinie fizyki wysokich energii, który dokonał się w ciągu ostatnich około osiemdziesięciu lat nie byłby możliwy bez znaczącego rozwoju w dziedzinie technik akceleratorowych i systemów detekcji cząstek. Najpotężniejszym z pracujących obecnie akceleratorów jest Wielki Zderzacz Hadronów (ang. Large Hadron Collider – LHC), znajdujący się w Europejskim Instytucie Badań Jądrowych (ang. European Organization for Nuclear Research – CERN). Usytuowany w tunelu o długości 27 km znajdującym się 100 m pod granicą szwajcarsko-francuską, miał w założeniu pozwalać na zderzenia przeciwbieżnych wiązek protonów o energii w układzie środka masy dochodzącej do 14 TeV[1].

Budowa akceleratora trwała prawie dwie dekady i pochłonęła blisko sześć miliardów franków szwajcarskich. Wynikiem międzynarodowej współpracy tysięcy naukowców i inżynierów z państw członkowskich CERN oraz państw-obserwatorów jest akcelerator wraz z czterema głównymi detektorami (A Toroidal LHC ApparatuS – ATLAS, ALICE, CMS i LHCb) umieszczonymi na jego obwodzie. Ze względu na złożoność projektu, montaż akceleratora i detektorów poprzedziły wieloletnie studia, których celem było opracowanie odpowiednich technologii, zaprojektowanie i przetestowanie poszczególnych elementów całego systemu.

Obecnie rozważana jest rozbudowa LHC mająca na celu dziesięciokrotne zwiększenie jego świetlności. Projekt nazwany LHC Wysokiej Świetlności (ang. High Luminosity LHC) dałby możliwość zbadania obszarów fizyki będących poza zasięgiem obecnie działającej maszyny. Szacuje się, że zwiększenie świetlności LHC zwiększy jego potencjał badawczy o około 20 % – 30 % w zakresie badań nad ciężkimi obiektami. Pozwoli także na bardziej precyzyjne wyznaczenie parametrów Modelu Standardowego, jak również dokładną weryfikację potencjalnych, nowych odkryć dokonanych dzięki LHC.

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[1] Energia osiągana obecnie przez LHC jest o połowę niższa od zakładanej na początku projektu i wynosi 7 TeV w układzie środka masy. LHC daje również możliwość przyspieszania ciężkich jonów, między innymi ołowiu $^{208}Pb^{82+}$.

Niezwykle ważną częścią obecnego, jak również zmodernizowanego eksperymentu ATLAS jest detektor wewnętrzny (ang. Inner Detector – ID), którego część stanowi krzemowy detektor śladowy (ang. Semiconductor Tracker – SCT). W związku z programem podwyższenia świetlności LHC detektor wewnętrzny będzie wymagał wymiany za około 10 lat. Przyszły detektor będzie składał się w całości z sensorów krzemowych, pikselowych i paskowych.

Jednym z wielu wyzwań stojących przed inżynierami pracującymi nad stworzeniem nowego SCT jest budowa systemu dystrybucji mocy dla elektroniki odczytu. W tym miejscu należy zauważyć, że aby zapewnić poprawne działanie detektora wewnętrznego w warunkach podwyższonej świetlności, konieczne jest dziesięciokrotne zwiększenie liczby kanałów odczytowych. Ma to przede wszystkim zagwarantować lepszą przestrzenną zdolność rozdzielczą, a co za tym idzie, pozwolić na dokładniejszą identyfikację torów cząstek produkowanych w wyniku zderzeń. Konsekwencją takiego stanu rzeczy będzie zwiększone zapotrzebowanie na moc dostarczoną do detektora.

Istnieje jednak szereg ograniczeń, które przy budowie systemu zasilania elektroniki w przyszłym detektorze, narzucają konieczność zastosowania nieco bardziej niekonwencjonalnych metod niż ma to miejsce w obecnie działającym SCT. Przede wszystkim liczba kabli dostarczających moc do obecnego detektora jest ściśle ograniczona i nie może być zwiększona, gdyż jest ”zaszyta” wewnątrz kriostatu oraz kalorymetrów. Instalacja nowych kabli prowadziłaby do zwiększenia masy detektora, co oznaczałoby degradację jego parametrów związanych ze śledzeniem torów cząstek.

Obecnie rozważa się dwa odmienne podejścia do realizacji systemu dystrybucji mocy w przyszłym detektorze SCT. Są to system szeregowego zasilania modułów detektora przy użyciu zewnętrznego źródła prądowego oraz równoległe zasilanie modułów przy pomocy wysokiego napięcia, zakładające dwustopniową konwersję mocy na poziomie pojedynczych modułów i układów scalonych z elektroniką odczytu.

Obydwie przedstawione powyżej opcje zakładają użycie przetworników (konwerterów) mocy DC-DC, pracujących w oparciu o przełączane pojemności. System szeregowego zasilania modułów detektora wymaga dodatkowo zastosowania liniowego regulatora napięcia w celu dostosowania wartości i jakości napięcia zasilania do wymagań analogowej elektroniki odczytu.

Rozdział pierwszy niniejszej pracy zawiera specyfikację proponowanych systemów dystrybucji mocy, jak również opis obecnego detektora ATLAS i plany dotyczące jego modyfikacji w przyszłości, związane z programem podwyższania świetlności akceleratora LHC. Natomiast główną część pracy stanowi opis wspomnianych, kluczowych elementów systemów dystrybucji mocy, proponowanych dla przyszłego detektora SCT,

czyli konwerterów mocy oraz liniowych regulatorów napięcia.

Wraz ze wzrostem świetlności akceleratora, znacznie zwiększy się dawka promieniowania w obszarze detektora wewnętrznego, co narzuca dodatkowe wymaganie dla elektronikę – odporność na radiację. Aby sprostać temu wymaganiu konieczne jest wykonanie testów radiacyjnych, które pozwolą poznać ograniczenia technologii i ocenić jej przydatność w realizowanym projekcie.

Obecnie zakłada się, że technologia IBM CMOS 130 nm jest najpoważniejszym kandydatem do zastosowania w projekcie nowej elektroniki odczytu dla SCT. Na pewnym etapie prac nad detektorem, rozważano również użycie nowszej technologii IBM CMOS 90 nm. Rozdział drugi zawiera opis struktur testowych użytych do testów radiacyjnych wraz z uzyskanymi rezultatami. W celu scharakteryzowania danego procesu technologicznego badano ewolucję podstawowych parametrów tranzystorów (napięcie progowe, transkonduktancja, prąd upływu, rezystancja załączenia, itd.) w funkcji całkowitej dawki promieniowania. Wyniki otrzymane z testów obydwu technologii zostały porównane, a doświadczenie zdobyte podczas analizy danych otrzymanych z naświetlań struktur testowych wykonanych w technologii 130 nm zostało wykorzystane podczas projektowania układów elektronicznych opisanych w dalszej części rozprawy.

W pracy opisane zostały dwie architektury konwerterów mocy opartych na przełączanych pojemnościach. Przetworniki te można scharakteryzować przy pomocy tzw. współczynnika konwersji, który definiuje się jako stosunek napięcia wyjściowego do napięcia wejściowego. Pierwszym z omawianych układów jest pompa ładunkowa ze współczynnikiem konwersji równym 2. Pozwala ona uzyskać napięcie dwukrotnie wyższe od napięcia zasilania. Drugi konwerter, o współczynniku konwersji $1/2$, daje możliwość dwukrotnego obniżenia napięcia wejściowego. Oba omawiane prototypy układów, umieszczone na prototypowym układzie scalonym DCDC013, zostały zaprojektowane i wykonane w technologii CMOS 130 nm. Podczas fazy projektowej szczególny nacisk położony został na optymalizację konwerterów w celu uzyskania ich jak najwyższej sprawności energetycznej. Omawiane konwertery planuje się w przyszłości zintegrować na układzie scalonym ABCN-13 z elektroniką odczytu. Rozdział trzeci niniejszej pracy doktorskiej zawiera opis zastosowanych architektur, wyniki symulacji komputerowych i testów prototypowych układów scalonych oraz rezultaty testów radiacyjnych.

W ostatniej części pracy przedstawione zostały dwa projekty liniowych regulatorów napięcia: klasyczny, oparty na tranzystorze polowym z kanałem typu *n* oraz tzw. liniowy regulator napięcia typu Low-Dropout, oparty na tranzystorze z kanałem typu *p*. Prototypy obu regulatorów zostały wykonane jako układ scalony VREG013 i podobnie jak omawiane wcześniej konwertery mocy, zostały zaimplementowane w technologii

IBM CMOS 130 nm. Zadaniem regulatora napięcia w tej architekturze jest poprawienie jakości napięcia zasilania części analogowej chipu ABCN-13 poprzez filtrację tętnień pochodzących z ładowania i rozładowywania pojemności wyjściowej pompy ładunkowej. W pracy przedstawiono opis architektur zastosowanych przy projektowaniu stabilizatorów napięcia z uwzględnieniem zastosowanych wzmacniaczy błędu. Szczegółowo omówione zostały również wyniki symulacji komputerowych, pomiarów prototypowych układów oraz wyniki otrzymane podczas testów radiacyjnych.

Contents

List of Acronyms

ABCN-13	ATLAS Binary Chip Next designed in 130 nm CMOS technology
ABCN-25	ATLAS Binary Chip Next designed in 250 nm CMOS technology
AC	Alternating Current
ALICE	A Large Ion Collider Experiment
ASIC	Application Specific Integrated Circuit
ATLAS	A Toroidal LHC Aparatus
BiCMOS	Bipolar CMOS technology
CBC	CMS Binary Chip
CCD	Charge-Coupled Device
CERN	Conseil Européen pour la Recherche Nucléaire
CMOS	Complementary Metal-Oxide Semiconductor
CMS	Compact Muon Solenoid
CNGS	CERN Neutrinos to Gran Sasso
COMPASS	Common Muon and Proton Apparatus for Structure and Spectroscopy
CSC	Cathode Strip Chamber
DC	Direct Current
DRC	Design Rule Check
DESY	Deutsches Elektronen Synchrotron
DUT	Device Under Test
ELT	Enclosed Layout Transistor
ENC	Equivalent Noise Charge
ESR	Equivalent Series Resistance
FET	Field-Effect Transistor
FCal	Forward Calorimeter
GBT	GigaBit Transceiver
GEM	Gas Electron Multiplier
HCC	Hybrid Controller Chips
HEP	High Energy Physics
HERA	Hadron-Electron Ring Accelerator
HL-LHC	High Luminosity LHC
IBM	International Business Machines Corporation
IBL	Insertable *B*-Layer
ID	Inner Detector
IP	Interaction Point
LDO	Low Drop-Out

LEIR	Low Energy Ion Ring
LEP	Large Electron Positron Collider
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LHCf	Large Hadron Collider forward
MDT	Monitored Drift Tube
MoEDAL	Monopole and Exotic Detector At the LHC
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MOS	Metal-Oxide Semiconductor
MSSM	Minimal Supersymmetric Standard Model
NFET	N-channel Field-Effect Transistor
NIEL	Non-Ionizing Energy Loss
NMOS	N-channel Metal-Oxide Semiconductor transistor
PCB	Printed Circuit Board
PFET	P-channel Field-Effect Transistor
PMOS	P-channel Metal-Oxide Semiconductor transistor
PS	Proton Synchrotron
PSB	Proton Synchrotron Booster
PSRR	Power Supply Rejection Ratio
QCD	Quantum Chromodynamics
QGP	Quark-Gluon Plasma
RAL	Rutherford Appleton Laboratory
RF	Radio Frequency
RFQ	Radio-Frequency Quadrupole
RHIC	Relativistic Heavy Ion Collider
RHP	Right Half-Plane
RMS	Root Mean Square
RPC	Resistive Plate Chamber
SC	Switched Capacitor
SCC	Stave Controller Chip
SCT	Semiconductor Tracker
SEE	Single-Event Effect
SEU	Single-Event Upset
SPS	Super Proton Synchrotron
SM	Standard Model
SMD	Surface Mount Device
SMU	Source Monitoring Unit
SPICE	Simulation Program with Integrated Circuit Emphasis
STI	Shallow Trench Isolation
SUSY	Supersymmetry
TGC	Thin Gas Chamber
TID	Total Ionizing Dose
TOTEM	Total cross section, Elastic scattering and diffraction dissociation Measurement at the LHC

TR	Transition Radiation
TRT	Transition Radiation Tracker
VBF	Vector Boson Fusion

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Introduction

Since the ancient times philosophers and scientists have been trying to develop a complete theory that could give the answer to the fundamental questions about the origin of the Universe and structure of matter. Although such a universal theory still remains unreachable, there are models that give us a general overview of the world that surrounds us. One of these theories is the Standard Model (SM) developed in early 1970s by Steven Weinberg, Sheldon Glashow and Abdus Salam. It successfully explains the results obtained from High Energy Physics (HEP) experiments and also predicts a wide spectrum of physics phenomena. Over the last forty years this mathematical model describing fundamental particles and their interactions has become a well-tested physics theory.

Although the SM presents a very condense and compact description of matter and interactions is also has limitations, mainly the gravitational interaction, massless neutrinos and spontaneous breaking of electroweak symmetry (a so-called Higgs mechanism). In order to investigate this phenomena physicists use powerful particle accelerators equipped with sensitive and precise detector systems. Currently, the most powerful accelerator is the Large Hadron Collider (LHC) located at European Organization for Nuclear Research CERN, the world's largest particle physics laboratory.

The protons or heavy ions accelerated in the LHC collide inside the large experiments (ATLAS, ALICE, CMS and LHCb), equipped with sophisticated tracking systems and calorimeters. Although the LHC and the experiments located on its perimeter are currently operating and collecting data from these collisions, physicists and engineers are considering an upgrade that will allow better use of the potential given by the accelerator.

In case of the ATLAS experiment the upgrade scenario assumes a significant intervention in the ATLAS Semiconductor Tracker (SCT). However, taking into account the complexity of the detector, its upgrade must be preceded by numerous Research and Development (R&D) projects and all possible scenarios must be investigated. The tracker is an essential part of the entire detector and a heart of the experiment, and its upgrade is essential for future performance of the ATLAS detector. The increase in the number of the readout channels will require more power, which has to be delivered to

the front-end electronics using the existing cable infrastructure. Thus, new solutions for the powering scheme must be elaborated. Currently, two possible approaches, a serial powering and a parallel powering scheme using the DC-DC conversion technique, are under development.

The main objective of this thesis is to develop the prototype designs of the radiation tolerant building blocks, which in the future will be implemented in the power distribution systems proposed for the upgraded ATLAS SCT. The dissertation presents four designs, namely a switched capacitor DC-DC step-up converter and two different architectures of linear voltage regulators, planned to be used in the serial powering scheme, and a switched capacitor DC-DC step-down converter, foreseen to be implemented in the parallel powering scheme. All the circuits listed above were designed and manufactured in the IBM 130 nm CMOS process[1].

However, before the design phase starts, it is important to investigate the radiation tolerance of the technology itself. This will obviously help to avoid any unexpected behaviour of the electronic circuits installed the future detector. One should keep in mind that the SCT front-end electronics will have to operate close to the interaction point, in a very high radiation field.

Thus, Chapter 2 describes the irradiation tests performed on dedicated CMOS structures fabricated in the IBM 130 nm technology node, the main candidate for the electronics upgrade in the SCT and the IBM 90 nm process, considered to be a backup option. During the tests the radiation induced evolution of the basic MOS transistor parameters (threshold voltage, leakage current, etc.) has been monitored. The final TID reached in the experiment varies between 50 Mrad and 200 Mrad, which corresponds to the expected TID value after the High Luminosity Upgrade in the SCT region.

The development of the new powering scheme is a crucial step in the SCT upgrade process and it requires a design of radiation tolerant building blocks, which will be implemented into the future front-end chip. In both cases, serial and parallel powering scheme, switched capacitor DC-DC converters are planned to be used. In the serial powering scheme the clean supply voltage for the analogue front-end electronics must be produced from the lower voltage provided by the shunt voltage regulator. This can be done using a switched capacitor DC-DC step-up converter. In the second scheme, the supply voltage for the digital part of the read-out chip will be produced from a higher voltage by the switched capacitor DC-DC step-down converter. The designs of these converters are driven by the power efficiency, thus the design must be preceded by analysis of the

[1]Complementary Metal-Oxide Semiconductor (CMOS) 8RF is a process with 130 nm lithography node, providing 8 metal levels and characterised for operation at both supply voltages, 1.2 V and 1.5 V

power losses occurring in the switching MOS transistors. Both designs are characterised by high power efficiency obtained for the required values of the load currents. They have been implemented in the DCDC013 chip, fabricated in 130 nm CMOS technology. Chapter 3 contains the design considerations, performance and irradiation test results of these two circuits.

In the serial powering scheme, the output voltage from the switched capacitor DC-DC step-up converter has to be lowered in order to meet the specification for the analogue front-end electronics. The quality of this voltage is poor, because of the voltage ripple occurring due to the capacitor charging and discharging. Therefore, the step-up converter must be followed by a linear voltage regulator. The author of this thesis was responsible for the development of two prototypes of linear voltage regulators, which have been implemented on the VREG013 chip and manufactured in the same technology node as the DC-DC converters. Two different architectures have been investigated and are presented in Chapter 4, a classical design based on a *n*-channel transistor as a pass element and an Low Drop-Out (LDO) voltage regulator architecture employing a *p*-channel device. The architectures of the prototypes, together with the pre- and post-irradiation test results are presented and discussed.

Chapter 1

Present and future High Energy Physics experiments at the LHC

1.1 Large Hadron Collider

The concept of a modern particle accelerator design was presented in the mid-forties of the last century by a Russian experimental physicist, Vladimir I. Veksler. His innovative ideas led finally to the development of a synchrotron. Within the next sixty years great progress in the field of accelerator technology has been made. This resulted in the development of several new accelerator facilities around the world, e.g. Large Electron Positron Collider (LEP) (a lepton-lepton collider, operating from 1989 to 2000) at CERN, Hadron-Electron Ring Accelerator (HERA) (a lepton-hadron collider, 1992 – 2007) at DESY and Tevatron (a hadron-hadron collider, 1983 – 2011) at Fermilab.

The great discoveries in the field of HEP made during the last three dacades, thanks to those machines (the discovery of the Z and the W bosons at LEP and the observation of the bottom quark at the Tevatron), led scientists to make another step on the way to recognising the nature of matter. This step was finally made in 1984, when it was decided that the LHC would replace LEP. In December 1994, a new proton-proton collider project was officially approved by the CERN Council. Simultaneously, numerous research and development (R&D) programmes, aiming at the development of technology allowing for the construction of the accelerator and the detectors, were started. Finally, on the 10^{th} of September 2008, after many years of construction and commissioning, the first beam was successfully circulated in the LHC. Unfortunately, a few days later an accident shut the collider down for over a year. The LHC was restarted in November 2009 and low-energy beams were injected and circulated in the beam pipes for the first time since the accident

occurred. On the 30th of March 2010, first collisions of proton beams at the energy of 7 TeV in the centre-of-mass took place. Since that time the LHC has been successfully operating with gradually increasing luminosity.

The Large Hadron Collider sits in a 27 km tunnel, formerly used as the facility for Large Electron Positron Collider. The LHC was designed to collide two opposing beams of protons of the nominal energy 14 TeV in the centre-of-mass or fully stripped lead ions, $^{208}Pb^{82+}$, of energy 2.76 TeV per nucleon (the total energy in the centre-of-mass of 1.15 PeV). A nominal beam of protons consists of 2,808 bunches and each bunch consists of $1.15 \cdot 10^{11}$ protons. The total energy of one circulating beam is around 362 MJ [1].

To keep the high energy beams on their track, 1,232 dipole superconducting magnets, are used. At the nominal beam energy the bending magnets containing superconducting coils, made of low-loss NbTi cable, can produce vertical magnetic field of 8.33 T at a current of 11.85 kA. During operation, the magnets must be constantly kept at a temperature of 1.9 K; superfluid helium is used as the coolant [2]. To keep the beams focused and their trajectories stable, 392 superconducting quadrupole magnets are used. The overall magnet system is complex and contains many other types of magnets, e.g. insertion magnets or corrector magnets (sextupole and decapole), mounted at the two ends of main dipoles to assure the quality of the magnetic field [3]. It is worth noting that in order to achieve the energies foreseen for the LHC beams, while using conventional magnets, the tunnel would have been 120 km long.

Beam acceleration is a complicated and multi-stage process. The proton and heavy-ions, injected to the LHC, must have initial energies of 450 GeV and 36.9 TeV, respectively [1]. This can be done thanks to the injection chain [4], used previously for the LEP and upgraded afterwards to meet strict requirements of the LHC machine, like many high intensity proton bunches with small transverse and well defined longitudinal emittances. The injection chain used for the proton-proton collisions consists of four stages: Linac-2, Proton Synchrotron Booster (PSB), Proton Synchrotron (PS) and Super Proton Synchrotron (SPS) [5].

- Linac-2 produces a 180 mA proton beam with an energy of 50 MeV from a duo-plasmatron source and supplies the PSB. Linac-2 consists of RFQ (Radio-Frequency Quadrupole, a linear accelerator structure for low-velocity ions) and three Alvarez tanks operating at 200 MHz [6].

- PSB improves the proton beam, accelerated up to a kinetic energy of 1.4 GeV. It consists of four vertically stacked synchrotron rings of 50 m in diameter. The four beams from the PSB are combined into one and sent, depending on the need, to the

Proton Synchrotron or to the ISOLDE[1] facility.

- PS is 628 m in circumference, consists of 277 conventional electromagnets. The PS allows proton beam acceleration up to 26 GeV. Using the Proton Synchrotron, it is also possible to accelerate electrons, heavy-ions (lead, sulphur, oxygen) and antiparticles (antiprotons and positrons).

- SPS is 6.9 km in circumference and operates up to 450 GeV. The SPS contains 1,317 conventional electromagnets, 744 of which are dipoles used to bend the beams around the ring. It is mainly used as the final injector for the LHC, however it also provides beams for the Common Muon and Proton Apparatus for Structure and Spectroscopy (COMPASS) experiment and the CERN Neutrinos to Gran Sasso (CNGS) project.

These elements of the acceleration chain have been working for many years before the concept of the LHC, thus all of them need to be upgraded to meet the strict requirements imposed by the LHC specification, i.e. production of bunches with 25 ns spacing, increase of the beam energy and intensity while maintaining stable high density bunches during the process of acceleration.

The LHC scientific programme also foresees Pb-Pb collisions. The ion injector chain is different from the proton chain described above, and consists of following elements: Linac-3, LEIR, PS, SPS, which supplies the LHC with 592 bunches, each of $7 \cdot 10^7$ lead ions [7]. The elements of the proton and heavy-ion acceleration chain are shown in Fig. 1.1.

1.1.1 The LHC experiments

The proton beams intersect in four points located on the LHC ring. In these places, called Interaction Points (IPs), the four main LHC experiments are placed. The two biggest ones, ATLAS and CMS, are general-purpose detectors aiming mainly at searching for the Higgs boson, supersymmetry and exotic particles. Two mid-size experiments, ALICE and LHCb, aim to study phenomena related to ion collisions and *B*-physics, respectively.

- **ATLAS** (**A T**oroidal **L**HC **A**pparatu**S**) is a general-purpose detector, the largest among all the LHC experiments. The detector will be described in more detail in Section 1.2.

[1] On-Line Isotope Mass Spectrometer, also know as ISOLDE Radioactive Ion Beam Facility is dedicated to producing radioactive nuclei and also to study of their properties.

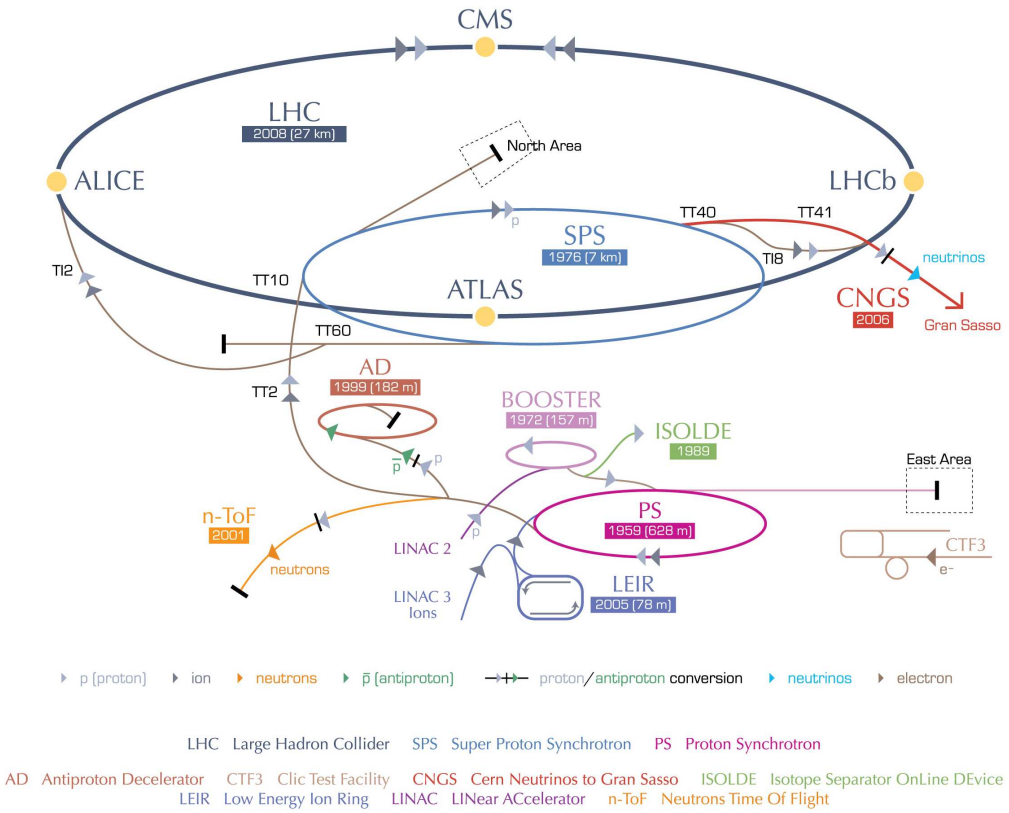

Figure 1.1: The LHC acceleration complex (reproduced from [8]).

- **CMS** (**C**ompact **M**uon **S**olenoid) is the second biggest LHC experiment (21.5 m long, 15 m in overall diameter and weighs 12,500 t). Similarly to ATLAS, it is a general-purpose experiment, which covers a wide spectrum of LHC physics. The main objective is to observe the Higgs boson, but the experiment also aims to search for supersymmetric particles, dark matter, string theory and extra dimensions. The CMS detector is built out of several layers. The inner part consisting of the silicon tracker, the electromagnetic and hadronic calorimeters is surrounded by the superconducting solenoid magnet generating magnetic field of 4 T. The outermost layer comprises the iron return yoke interspersed with the muon chambers [9].

- **LHCb** (**L**arge **H**adron **C**ollider **b**eauty experiment) is a single-arm spectrometer which stretches 19.7 m along the beam pipe. The detector is designed to exploit B- and $\bar{B}$-mesons produced with a boost relative to the laboratory reference frame. This boost combined with high-precision vertex reconstruction permits the study of asymmetries between B and $\bar{B}$. The nominal luminosity for the LHCb experiment should be kept at the level of $2 \cdot 10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, which however does not exclude the

increase of the nominal luminosity in the rest of Interaction Points [10].

- **ALICE** (**A** **L**arge **I**on **C**ollider **E**xperiment) is the last of the main LHC experiments. The ALICE experiment was designed and optimised to study the physics of strongly interacting matter at extreme energy densities, Quark-Gluon Plasma (QGP). The studies will be performed during collisions of lead ions with centre-of-mass energy of 5.5 TeV per nucleon pair. The detector aims to study the properties of hot QGP, its dynamical evolution, the phenomena related to the phase transition of so-called rehadronisation and the evolution of the hadronic final state [11].

Apart from the four main LHC experiments described above there are three much smaller experiments located close to the interactions points, namely TOTEM, LHCf and MoEDAL. They are run by much smaller collaborations, but also make a significant contribution to the exploration of the LHC scientific programme.

1.1.2 New physics at the Large Hadron Collider

The Standard Model of particle physics is a theory developed in early 1970s by Steven Weinberg, Sheldon Glashow and Abdus Salam. It successfully explains the results obtained from many High Energy Physics experiments and also can predict a wide spectrum of physics phenomena. Over the last forty years, this mathematical model describing fundamental particles and their interactions has become a well-tested physics theory. The Standard Model assumes the Universe is made from a very limited number of structureless particles [12], 6 leptons (carrying a unity electric charge, e) and 6 quarks (carrying fractional charges of $+2/3|e|$ and $-1/3|e|$). The model also includes fundamental interactions (or fields), described by the exchange of characteristic bosons: strong, electromagnetic and weak.

Although the Standard Model presents a very condense and compact description of matter, it has some weaknesses [13] and thus it cannot be considered as a final theory. The main weaknesses of the Standard Model are listed below:

1. The model does not explain some of the particle quantum numbers (electric charge, weak isospin, hypercharge and colour).

2. It contains 19 arbitrary parameters (including three independent gauge couplings and a possible CP-violating strong-interaction parameter, six quark and three charged-lepton masses, three generalised Cabibbo weak mixing angles and the CP-violating Kobayashi-Maskawa phase and finally, two independent masses for weak bosons).

3. An additional 9 parameters must be incorporated into the model in order to explain the neutrino oscillations (three neutrino masses, three real mixing angles, and three CP-violating phases) and more parameters will have to be added to generate masses for all neutrinos. One should note the Standard Model assumes that the neutrinos are massless.

4. The Standard Model does not incorporate gravitational interactions and all attempts for their inclusion in the model have failed so far.

The excellent parameters (collision energy, luminosity, etc.) of the Large Hadron Collider, together with very accurate detection systems guarantee a very broad physics programme and allow us to reach an energy spectrum not available before either at Tevatron or LEP.

The primary goal of the LHC project is to investigate the spontaneous symmetry breaking, which is essential for testing the Standard Model. This theory postulates the existence of a scalar boson (Higgs boson) which has not been observed yet. Another important goal is to detect superparticles, which will ultimately lead to the discovery of Supersymmetry (SUSY). Many other research areas will be investigated within the LHC scientific programme, namely the search for new physics beyond the Standard Model and the Minimal Supersymmetric Standard Model (MSSM)[2], *B*-physics, heavy-ion physics, top quark physics, QCD and electroweak interactions. The cross-sections and expected event rates for some of the Standard Model processes, Higgs boson production and supersymmetry are shown in Fig. 1.2.

Search for the Standard Model Higgs boson

The search for spontaneous symmetry breaking in the electroweak sector of the Standard Model is the primary objective of the LHC project. The theory of the Standard Model assumes that elementary particles mediating weak interactions, W boson and Z bosons, are massless. However, in 1983, two High Energy Physics experiments, UA1 and UA2, running on the Super Proton Synchrotron at CERN, reported the discovery of the W and Z bosons. Their masses were measured to be around 80.4 GeV and 91.2 GeV, respectively for W and Z. The discovery led to the Nobel Prize being awarded to Carlo Rubbia and Simon van der Meer, and it also became a major deviation from the theory. In order to overcome this problem, spontaneous symmetry breaking combined with so-called Higgs

[2]MSSM is a minimal extension to the Standard Model proposed in 1981. It realises the supersymmetry, assumes that each particle from the SM has its heavy superpartner (e.g. squarks, gluinos, sleptons).

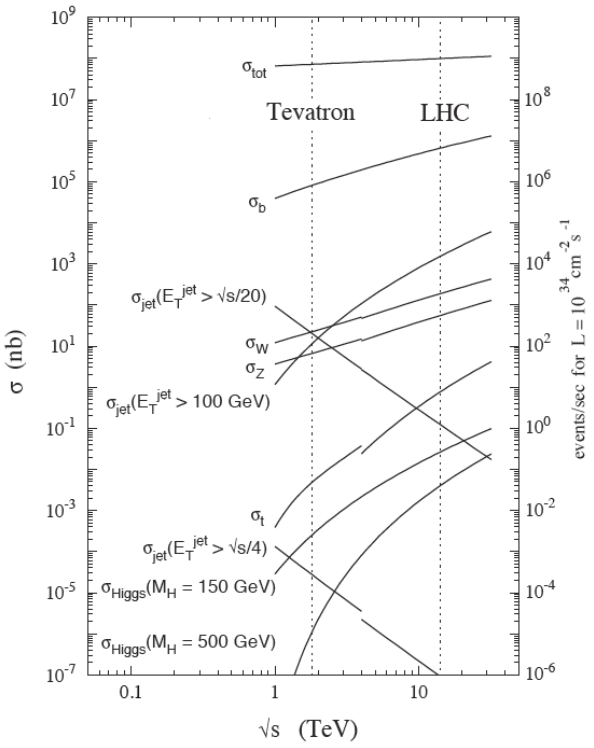

Figure 1.2: Cross-section and event rates for various processes in proton–(anti)proton collisions as a function of the centre-of-mass energy $\sqrt{s}$, at design luminosity of Tevatron ($\sqrt{s} = 1.96\,\text{TeV}$) and LHC ($\sqrt{s} = 14\,\text{TeV}$) [14].

mechanism was postulated. This theory requires the existence of a massive elementary particle, Higgs boson, which explains the inconsistencies between theoretical model and the experimental data. The Higgs boson would explain the difference between the massless photons, which mediate electromagnetic interactions, and heavy W and Z bosons mediating the weak forces.

Some of the energy regimes however have been excluded by LEP and Tevatron with a 95 % confidence level. LEP excluded mass below 114 GeV. The Fermilab experiments excluded the masses range between 158 GeV and 175 GeV. In the LHC the search for the Higgs boson will be made in the range from 110 GeV to 600 GeV.

The main Higgs boson production mechanism at the energies available at the LHC will occur mainly by gluon-gluon fusion ($gg \rightarrow H$) or Vector Boson Fusion (VBF) process ($gg \rightarrow ggH$). The processes like weak vector bosons ($q\bar{q} \rightarrow W/ZH$) or associated production with top quark pairs ($gg,\, q\bar{q} \rightarrow t\bar{t}H$) are characterised with much smaller cross-sections compared to the first ones [15]. The main search channels of the Higgs boson decays are as follows [16]:

- $H \to \gamma\gamma$ is a good candidate for the search of Higgs boson in low mass region, namely 114 GeV (just above the LEP limit) up to around $140 - 150$ GeV;
- $H \to ZZ^* \to 4\ell$ represents so-called "golden" channel. ZZ^* decay into 4 muons, 4 electrons or 2 muons and 2 electrons. This channel is expected to search for quite a wide range of Higgs boson mass, between 120 GeV and 600 GeV;
- $H \to \tau\tau$ in VBF events seems to be one of the most important channels, in which the Higgs bosons are radiated out by Z or W bosons exchanged between the interacting particles. The final states in the channel are: $\ell\ell$, ℓh and hh;
- $H \to WW^*$ is an important channel for the search of the Higgs mass range between 125 GeV and 190 GeV. There are two different final states taken into account for this channel: $\ell\ell\nu\nu$ and $\ell\nu jj$ ($\ell\nu qq$);
- $H \to b\bar{b}$ decay does not allow the observation of Higgs bosons, due to a very high background. However the observation is possible in associated process $gg,\ q\bar{q} \to t\bar{t}H$. The analysis of this case is difficult due to complex final state, which is as follows: $t\bar{t}H \to \ell\nu qq' b\bar{b}b\bar{b}$.

Prospects for supersymmetry within the MSSM

SUSY is an extension of the Standard Model in order to solve the hierarchy problem. It assumes that for high energies (around 1 TeV) there should be a symmetry between fermions and bosons, i.e. every particle would have a heavy superpartner. The symmetry is not exact, otherwise SUSY particles would have mass exactly the same as the original particles. The most commonly used supersymetric model is the Minimal Supersymmetric Standard Model. The list of particles and sparticles postulated by the MSSM theory is presented in Table 1.1.

An interesting thing is that the MSSM assumes the existence of five Higgs particles, scalar particles h^0 and H^0, pseudoscalar A^0 and two charged scalar particles H^+ and H^-.

The ATLAS and CMS experiments should be able to detect the signatures of superparticles like squarks or gluinos, if their masses are in the range of few TeV (up to around 2.5 TeV). Some scenarios of SUSY particle production in proton-proton collisions and their decays in the detectors have been simulated and accurately investigated. As a result from these studies, the selection of the required cuts for SUSY events has been done. High transverse-momentum p_{T} jets, together with large missing energy $E_{\mathrm{T}}^{\mathrm{miss}}$, the production of a certain number of electrons (e) and / or muons (μ) and decays of tau particles (τ) or b-quarks [17] may indicate evidence for the sparticles.

Table 1.1: Particles and their superpartners in MSSM [12].

Particle	Spin	Sparticle	Spin
quark q	$1/2$	squark $\tilde{q}$	0
lepton ℓ	$1/2$	slepton $\tilde{\ell}$	0
photon γ	1	photino $\tilde{\gamma}$	$1/2$
gluon G	1	gluino $\tilde{G}$	$1/2$
$W^{\pm}$	1	wino $\tilde{W}^{\pm}$	$1/2$
Z^0	1	zino $\tilde{Z}^0$	$1/2$

Heavy-ion physics

An extensive heavy-ion scientific programme is planned for three of the main LHC experiments, ALICE, ATLAS and CMS, but only the ALICE experiment is strictly dedicated to heavy-ion measurements. The nominal energy in the centre of mass foreseen for a Pb-Pb collision is 5.52 TeV per nucleon pair. This makes the LHC the highest energy heavy-ion collider in the world, almost 28 times more powerful than the Relativistic Heavy Ion Collider (RHIC) located in the Brookhaven National Laboratory. This gigantic research potential offered by the LHC machine will be used for studies of Quantum Chromodynamics (QCD), a fundamental theory of the strong interactions. The LHC programme includes studies for new phase of matter, QGP, produced in heavy-ion collisions, where huge energy density allows the transition towards partonic matter (the quarks and gluons are no longer confined within hardons). The heavy-ion physics programme also incorporates studies on elliptic flow phenomenon, jet quenching and the structure of the nucleus and nucleon.

New physics beyond the SM and MSSM

Studies concerning the search for extra dimensions, additional gauge bosons, heavy neutrinos, sgoldstinos, scalar leptoquarks, *R*-parity violation and additional Higgs bosons with large Yukawa coupling constants are also planned at the LHC experiments [18]. The probability of making a discovery in any of these exotic fields seems to be rather small, however if one is made, it will have a huge impact on our understanding of nature and will require modifying the laws of physics as we know them today.

1.2 ATLAS experiment

The ATLAS experiment must fulfil the following requirements [19] [20], in order to realise its scientific programme:

- very good electromagnetic calorimetry is necessary for the identification and measurement of photons and electrons, also good hadronic calorimetry is needed for precise measurements of jets and missing transverse energy ($E_{\mathrm{T}}^{\mathrm{miss}}$), especially important for SUSY particles searches,
- good muon identification and momentum measurement over a wide range of momenta,
- efficient tracking and high momentum resolution of charged particles in the Inner Detector, essential for τ-leptons and *b*-jet tagging and also for good secondary vertex reconstruction,
- large acceptance in pseudorapidity[3] (η) with almost full azimuthal angle coverage,
- efficient triggering and measurements of low transverse-momentum particles with good background rejection to enable reasonable trigger rate for the physics processed being in the LHC region of interest,
- fast, radiation-hard electronics and sensor elements in high granularity detector systems are needed due to harsh environmental conditions at the LHC.

1.2.1 The overview of the ATLAS detector systems

The ATLAS detector is located in IP 1, almost 100 m underneath the ground level in a $35 \times 55 \times 40\,\mathrm{m}^3$ cavern. The detector itself is 44 m long and 25 m in diameter. It weighs 7,000 tons and contains over 3,000 km of cables. This places ATLAS among the biggest detectors ever used in HEP experiments. The overall layout of ATLAS is shown in the Fig. 1.3. In the detector layout, one can distinguish three major sections: the Inner Detector (ID), mainly responsible for charged particles momenta measurements (described in section 1.2.2); the calorimetry system, measuring the energy carried by the particles and finally, muon spectrometer which identifies and measures the muons.

[3] Pseudorapidity is defined as $\eta = -\ln[\tan(\theta/2)]$, where θ is the relative angle to the $+z$ LHC beam axis.

In order to allow precise momentum measurements of the charge particles in the Inner Detector and the muon spectrometer, the presence of the magnetic field is absolutely required. Thus, the ATLAS experiment is equipped with the magnet system, which consists of the central solenoid, barrel toroid and two end-cap toroids.

There are also three subsystems, not visible in the presented layout, the trigger system, the data acquisition system and the computing system. They are responsible for processing the data collected during proton and ion collisions.

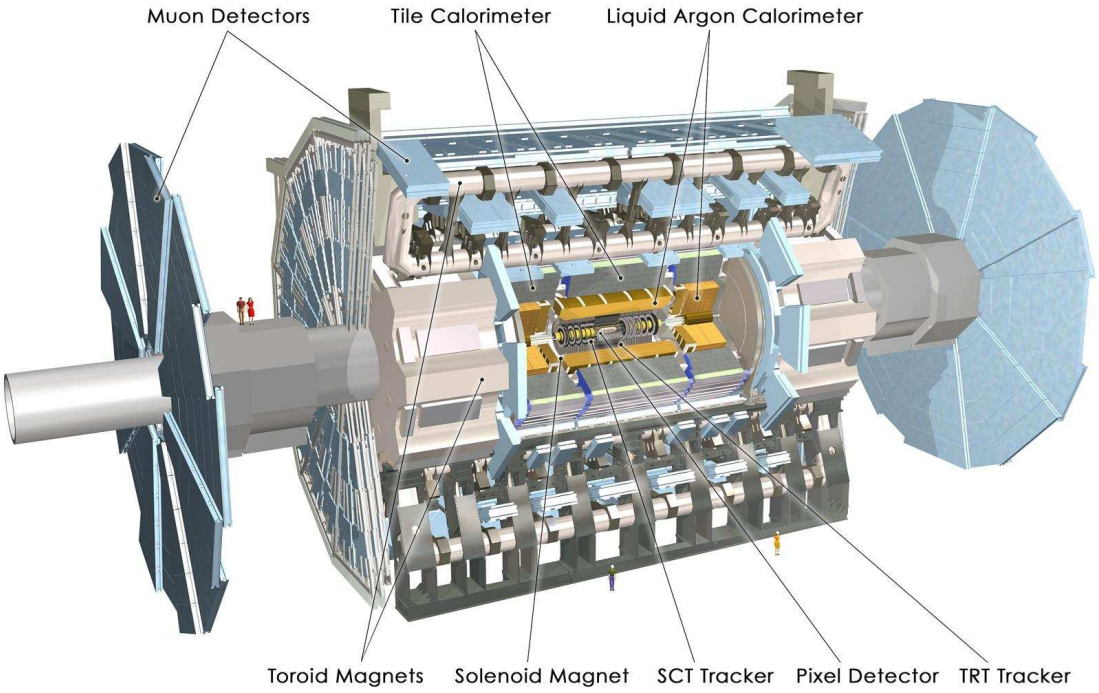

Figure 1.3: The overall view of the ATLAS detector (reproduced from [21]).

Calorimeter

In order to allow full reconstruction of the collision event, apart from excellent tracking and particle identification abilities, ATLAS must have possibility to make precise energy measurements. These measurements are made in a calorimeter, a block of matter in which the particles are fully absorbed due to their interaction with the medium. The result of that is a shower of secondary lower-energy particles. The deposited energy is finally transformed into charge, light or heat and detected by the active element [22].

ATLAS has two calorimeters, electromagnetic and hadronic, which cover a very wide range in pseudorapidity, $|\eta| < 4.9$. Different detection techniques are used and also

the granularity of the calorimeters is different depending on the physics process being investigated. High detector granularity in the central part allows precise measurements of photons and electrons, lower granularity in the other parts of detector is sufficient for jet reconstruction and $E_{\mathrm{T}}^{\mathrm{miss}}$ measurements. Also, the thickness of the detector must be sufficient to fully absorb the energy of the particle. Hence, the electromagnetic calorimeter was designed to have a thickness of more than 22 radiation lengths. The electromagnetic calorimeter is a lead and liquid argon (LAr) detector, where lead acts as an absorber and liquid argon, the sensing element. The hadronic calorimeter has a much more complex design using different materials as absorbers (steel, copper or tungsten) and as sensing elements (liquid argon or plastic scintillator) [23].

Muon Spectrometer

Muons are elementary particles, 207 times heavier than electrons, and due to that fact they do not emit as much bremsstrahlung radiation. Thus, muons of a given energy penetrate matter far more deeply than electrons, because they do not interact via the strong interaction with nuclei in the medium and their deceleration occurs mainly due to the energy lost by the bremsstrahlung mechanism.

The muon spectrometer was designed to allow momentum measurements over a very wide range of transverse momentum (p_{T}), pseudorapidity and azimuthal angle. The detector was designed in a way allowing muon identification up to $p_{\mathrm{T}} = 3\,\mathrm{GeV/c}$ and guarantees the momentum measurement up to values limited by the LHC.

The muon tracker is built around air core toroid magnets and organised in three barrels, concentric with respect to the beam pipe, and two end-caps. Together they provide a large coverage in pseudorapidity, $|\eta| < 2.7$. The muon spectrometer consists of four different types of gaseous detectors: Monitored Drift Tubes (MDTs), Cathode Strip Chambers (CSCs), Resistive Plate Chambers (RPCs) and Thin Gas Chambers (TGCs) [24]. The first two types are used for high precision muon tracking, while last two are a part of the ATLAS trigger system.

To provide the magnetic field, necessary for the muon spectrometer operation, the barrel toroid, consisting of eight superconducting $25\,\mathrm{m} \times 5\,\mathrm{m}$ size coils, is used. The coils are grouped and form a large toroidal shape of 22 m in diameter. Additionally, two end-cap toroids are placed inside the barrel toroid, on both sides of the ATLAS detector. Each end-cap, with a total weight of 239 t, consists of eight superconducting coils. The peak magnetic field obtained for the nominal current of 20.5 kA in the barrel toroid and end-cap toroids is 3.9 T and 4.1 T, respectively [25].

1.2.2 Inner Detector

The Inner Detector is placed in the centre of the ATLAS experiment, close to the beam pipe. It consists of three separate sub-detectors: the Pixel Detector, the Semiconductor Tracker, and the Transition Radiation Tracker (TRT). Together, they provide the tracking of charged particles for precise momentum measurement as well as primary and secondary vertex reconstruction in a pseudorapidity of $|\eta| \leq 2.5$. The ID also provides electron identification over a wide range of energies (between 0.5 GeV and 150 GeV) and pseudorapidity ($|\eta| \leq 2.0$). The Pixel Detector and the SCT are based on silicon pixel and strip detectors as active elements. The TRT consists of many layers of gaseous straw tubes which are interleaved with transition radiation foils. The entire tracker is surrounded by a solenoid, which provides a magnetic field of 2 T with a field direction parallel to the beam axis [26]. The full length of the combined inner tracker is more than 7 m, and the maximum radius is 1.08 m. The layout of the Inner Detector barrel is shown in the Fig. 1.4.

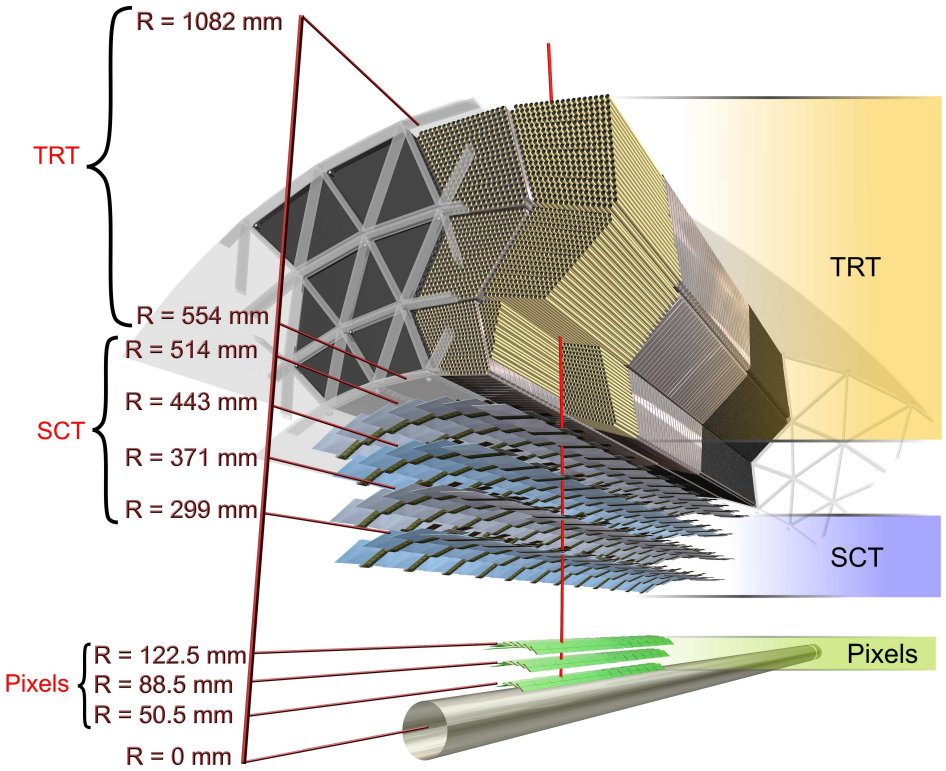

Figure 1.4: The cross-section of a fragment of the Inner Detector [23].

Pixel Detector

The ATLAS Pixel Detector is the innermost part of the ID. It provides high granularity and high precision measurements close to the interaction point. The pixel detector system is a very important part of the whole ATLAS detector and must comply with several strict requirements. Firstly, due to the fact that the pixel detector is placed very close to the interaction point, all its elements must be able to operate in a high radiation field. The predicted TID is around 500 kGy and Non-Ionizing Energy Loss (NIEL), $10^{15}\,1-\mathrm{MeV}$ equivalent neutrons per cm^2 ($\mathrm{n_{eq}\,cm^{-2}}$) over ten years of operation. Secondly the transverse space resolution must be better than 15 μm and the longitudinal resolution must be better than 1 mm to allow good primary vertex resolution measurements. Thirdly, the material budget in the pixel detector has to be minimised in order to decrease the rate of multiple scattering and other secondary interactions [27]. Finally, the pixel detector must guarantee excellent identification of jets originating from bottom quarks, e.g. Higgs boson decay into bottom quarks.

The pixel detector consists of a barrel and two identical end-caps. It is 1442 mm long and 430 mm in diameter. The barrel is built of three concentric layers at radii of 50.5 mm, 88.5 mm and 122.5 mm around the beam pipe. The end-caps in the forward and backward regions of the detector are identical and consist of three disks on each side, between radii of 88.8 mm and 149.6 mm. The Pixel Detector is built of 1,744 identical modules (1,456 modules in barrel region and 288 in end-caps) each with an active area of $6.08 \times 1.64\,\mathrm{cm}^2$. The sensors, produced in the radiation-hard n^+-in-n technology, are organised in 144 columns and 328 rows, which gives 47,232 pixel implants on each sensor tile. The sizes of pixel cells are different, $382.5 \times 30\,\mu\mathrm{m}^2$ and $582.5 \times 30\,\mu\mathrm{m}^2$, depending on the region on the sensor tile. In total, the Pixel Detector has over $8 \cdot 10^7$ read-out channels (over 67 million in the barrel and over 13 million in end-caps) and covers an area of around $1.7\,\mathrm{m}^2$.

One should note that the sensor leakage current and the operating voltage change with the total dose. After a fluence of around $2 \cdot 10^{13}\,\mathrm{n_{eq}\,cm^{-2}}$ n-type bulk material inverts to p-type. The effective doping in the silicon bulk grows with time and is temperature dependent. Hence, the sensors must be cooled down and operated at a temperature between $-5\,^\circ\mathrm{C}$ and $-10\,^\circ\mathrm{C}$ [23]. Fluorocarbon (C_3F_8) operating with a nominal temperature of $-25\,^\circ\mathrm{C}$ is used as a coolant.

Semiconductor Tracker

The SCT was designed to be hermetic for charged particles of transverse momentum higher than 1 GeV and to provide accurate tracking of charged particles produced in

proton-proton and ion-ion collisions. Its transverse space-point resolution is around 17 μm while the longitudinal resolution, around 580 μm. The SCT occupies radii between 30 cm and 52 cm from the beam axis, and spreads to ± 2.7 m along the beam pipe. The effective tracking coverage is $|\eta| \leq 2.5$.

Due to the fact that the SCT is located close to the interaction point, it must fulfil all the strict radiation hardness requirements. The NIEL is estimated to be around $2 \cdot 10^{14} n_{eq}\,cm^{-2}$ and TID around 100 kGy over a period of 10 years. In order to reduce the radiation damage effects and allow the sensors to survive over those years, the SCT must be cooled down. Thus, the end-caps to are cooled down to $-7\,^{\circ}$C and the inner layers of the barrel to around $-2\,^{\circ}$C. The detector support structure must also be non-magnetic due to the presence of magnetic field generated by the solenoid producing 2 T magnetic field [28] [29].

The SCT, like other ID sub-detectors, has a modular construction. It consists of three parts, the barrel and two end-caps, all located inside the solenoid. The total area of silicon used in the SCT barrel is $34.4\,m^2$. The SCT barrel is built of four cylindrical and concentric layers containing 2112 silicon modules covering $|\eta| \leq 1.3$. The modules consist of two single-sided silicon *p*-in-*n* (*p*-type strips on *n*-type silicon) sensors. In order to guarantee two-dimensional measurements, the sensors are glued back-to-back and slightly tilded (the angle is 40 mrad). Each sensor has 768 strips, which are 126 mm long, and are separated with a constant pitch of 80 μm [30]. The strips are read out by the front-end ABCD3TA chips, fabricated in BiCMOS radiation resistant technology. There are six read-out chips on each single-sided sensor, which gives the total number of $3.2 \cdot 10^6$ read-out channels in the SCT barrel.

The SCT end-caps are organised in eighteen disks (nine on each forward and backward side of the tracker) surrounding the beam pipe, covering an area of $26.7\,m^2$ with silicon. Each end-cap is built of 988 silicon modules mounted on the disks and organised in three rings: inner, middle and outer. To avoid the gaps in the detector, the sensors on each ring overlap [31]. The total number of read-out channels in the end-caps is $3 \cdot 10^6$, which totals $6.2 \cdot 10^6$ for the whole Semiconductor Tracker.

Transition Radiation Tracker

The idea of this detector is based on the theory of Transition Radiation (TR), a physics phenomenon predicted theoretically by Vitaly L. Ginzburg and Ilya M. Frank. The theory of TR says that photons are emitted when charged particles cross the boundary between two media with different dielectric constants [32]. The total energy and number of TR photons is proportional to the Lorentz factor (γ) of the particle. The total radiation

intensity can be written as follows [1.1]:

$$S_0 = \frac{\alpha\hbar}{3}\frac{(\omega_1-\omega_2)^2}{\omega_1+\omega_2}\gamma, \tag{1.1}$$

where ω_p and θ_p are the photon frequency and the angle of emission with respect to the particle trajectory, $\alpha = e^2/\hbar c \approx 1/137$ is the fine-structure constant and $\omega_{1,2}$ are the plasma frequencies of the two media [33]. Due to the simple relation between the total TR intensity and the Lorentz factor, the Transition Radiation Tracker can be used for particle identification, e.g. separation of electrons from heavier charged particles – muons and pions.

The TRT consists of three parts, a barrel and two end-caps. Its basic elements are thin-walled proportional drift tubes, called straw tubes or simply straws. Straw tubes were chosen as detecting elements because they offer a high degree in modularity of the detector and they can be easily integrated into a medium (polypropylene-polyethylene fibre mat) producing transition radiation without compromising the continuous tracking concept. The TRT straw layout is designed so that charged particle tracks with transverse momentum $p_T > 0.5\,\text{GeV}$ and with pseudorapidity $|\eta| \leq 2.0$ [34] cross about 35 straws providing continuous tracking at larger radii of the Inner Detector while enhancing its pattern recognition ability.

The barrel part is comprised of 52,544 straws oriented parallel to the beam. It covers the radius range $56-108\,\text{cm}$ and has a sensitive region of total length of 144 cm along the beam, corresponding to a pseudorapidity range of $|\eta| \leq 1.0$ [35].

Each of the two end-caps contains 122,880 straws radially aligned with respect to the beam axis. They cover the forward and backward pseudorapidity region, $1.0 \leq |\eta| \leq 2.0$. The full length of each end-cap is 1.9 m, the diameter is about 2.2 m and the weight is about $1,119\,\text{kg}$ [36].

1.3 High Luminosity Upgrade

In order to discuss the problem of the High Luminosity Upgrade, one has to understand the meaning of a key parameter know in HEP and the accelerators' technology as luminosity. Luminosity ($\mathcal{L}$) is a parameter, which allows us to estimate the number of particular events (N_{event}) per second produced in a collision. The cross-section for a particular event (σ_{event}) is usually taken from a theoretical model. This simple relation is show below (1.2):

$$N_{\text{event}} = \sigma_{\text{event}}\,\mathcal{L}, \tag{1.2}$$

The luminosity depends only on the beam parameters and is a combination (Eq. 1.3) of the following parameters [2]: the revolution frequency in the storage ring (f_{rev}), the relativistic Lorentz factor (γ), the normalised transverse emittance (ε_{n}), the beta function at the collision point (β^*) and finally, the number of particles per bunch and the number of bunches per beam (N_{b} and n_{b}), respectively.

$$\mathcal{L} = \frac{N_{\mathrm{b}}^2 \, n_{\mathrm{b}} \, f_{\mathrm{rev}} \, \gamma}{4 \, \pi \, \varepsilon_{\mathrm{n}} \, \beta^*} \, F(\phi_{\mathrm{P}}). \tag{1.3}$$

The value of the luminosity is modified by a geometric factor $F(\phi_{\mathrm{P}}) = 1/\sqrt{1+\phi_{\mathrm{P}}^2}$, where ϕ_{P} is the Piwinski angle [37].

The nominal peak luminosity in the LHC machine measured at IP1 (ATLAS) and IP5 (CMS) is assumed to reach $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ in case of proton beams and around $10^{27}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ for heavy ion beams. Currently, the LHC operates at lower energy (3.5 TeV per beam for protons) and the peak luminosity of $3.65 \cdot 10^{33}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, reached in 2011. The integrated luminosity recorded by the ATLAS experiment during the proton runs in 2010 and 2011 was $5.257\,\mathrm{fb}^{-1}$, so five times higher than expected at the beginning of 2010 [38].

1.3.1 High Luminosity Upgrade of the LHC

The studies for the High Luminosity Upgrade of the Large Hadron Collider were started several years ago and are still ongoing. It was foreseen that some parts of the LHC and the innermost parts of the detectors would start to suffer from radiation effects after several years of running. This will be a great chance to implement some technical improvements and several new elements in the detector system. The project considering these upgrades is called the High Luminosity LHC (HL-LHC) project and it aims at ten-fold increase of the nominal luminosity.

Among the most important issues which have to be investigated and solved in order to allow the luminosity increase, one can enumerate the following: increase of the number of collisions per bunch crossing, decrease of the beta function (β^*) at the collision point, development of the new final-focus quadrupoles, improvement of the LHC injection chain due to higher beam current, upgrade of the collimation system, increase of the magnet lifetime in a high-radiation field and some additional improvement in shielding. The HL-LHC project is divided into two phases:

Phase I of the High Luminosity Upgrade assumes the increase of the luminosity up to $1-2 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and it is foreseen for 2017. This will be achieved by incorporating

Linac-4 in the LHC injection chain, providing an intensity of $1.7 \cdot 10^{11}$ protons per beam. Linac-4 will be ready in 2014 and it will work as the injector for the PSB, increasing its brightness by a factor of two with 25 ns bunch spacing. The beam focusing in IP1 and IP5 will be improved by replacing of the inner triplet quadrupole magnets focusing the beam by new NbTi ones, new separation dipoles and new front quadrupole absorber [39]. Thanks to these improvements the integrated luminosity of $320\,\mathrm{fb}^{-1}$ until 2020 is expected.

Phase II of the machine upgrade is expected in 2021 and will incorporate serious changes in the injection chain, which should allow for the ultimate luminosity of $5 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. After Phase II the LHC should achieve $250\,\mathrm{fb}^{-1}$ per year, resulting in $3000\,\mathrm{fb}^{-1}$ in 12 years of operation. The upgrade of the Proton Synchrotron Booster up to energy of 2 GeV is seriously considered, as well as the Super Proton Synchrotron upgrade. There are also plans aiming for further beam parameters improvement by using new Nb_3Sn triplet quadrupole magnets. The luminosity ($\mathcal{L}$) can be also be increased by tweaking the values of the beam crossing angle and / or the bunch length (see Eq. 1.3). Currently, a so-called crab crossing collision scheme is considered as a baseline for the luminosity increase for the HL-LHC [40].

1.3.2 Physics beyond the LHC

The detailed physics programme of the HL-LHC will be highly dependent on the results obtained from the experiments operating at the LHC. As such, it would be very difficult to predict about the detailed prospects for physics at the HL-LHC. Nevertheless, some extensive studies in this field are ongoing. The High Luminosity Upgrade should increase the LHC discovery reach by between 20 % and 30 % in terms of the mass of new objects [41]. Also the measurement precision will be significantly improved. Hence, even the statistics-limited phenomena like Higgs Self-Coupling or rare decays (e.g. $H \rightarrow \mu\mu$) should be observed and measured with a reasonable accuracy.

If we assume that the main part of the LHC scientific programme (see section 1.1.2), related with the search for the Higgs boson and Supersymmetry is realised, then one can divide the HL-LHC scientific programme into the following topics [42]:

- further improvement of the accuracy in determination of Standard Model parameters (e.g. Higgs couplings),

- more accurate measurements of the parameters describing new physics discovered at the LHC (e.g. supersymmetry particles),

- new discoveries in the high-mass region (e.g. quark compositeness, new heavy gauge bosons, multi-TeV squarks and gluinos, extra-dimensions),
- extension of the sensitivity to rare processes (e.g. Higgs-pair and multi gauge boson production).

1.3.3 High Luminosity Upgrade of the ATLAS detector

Due to the fact that the innermost parts of the ATLAS detector are located in a very high radiation field, their lifetime is strictly limited. A ten-fold increase of the nominal luminosity after the upgrade to the HL-LHC will drastically increase the level of radiation.

The limited functionality of the current Inner Detector is mainly related to the limited radiation hardness of the silicon detectors. The radiation induced reduction in the depletion depth and ultimate charge trapping may result in the loss of signal from the detectors. The increase of the leakage current is also a big issue. Not only will the silicon sensors suffer from high radiation, the front-end electronics and data transmission systems will also be affected.

The radiation damage is not the only issue enforcing changes in ATLAS. The increase of the luminosity means the increase of the number of proton-proton collisions per bunch crossing. The expected number of pile-up events per bunch crossing at the HL-LHC will be around 200. This is one order of magnitude higher than at the LHC and will result in a large detector occupancy. Figure 1.5 shows the increase in the number of tracks produced in 5 and 400 proton-proton collisions, corresponding to the luminosity of $0.2 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and $10 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, respectively. In order to provide the same detector performance, despite this tremendous increase of pile-up events per bunch crossing, an increase in the detector granularity is absolutely needed. Higher granularity is required to keep the occupancy at the level allowing efficient pattern recognition and thus providing a better physics analysis.

The ATLAS Inner Detector will not be the only sub-detector affected by the high dose rate. According to the simulations, all the detectors located at low radii and large pseudorapidity, like Forward Calorimeter (FCal) and forward muon wheels, will suffer from radiation damage and high occupancy.

Phase I of the High Luminosity Upgrade of ATLAS anticipates the replacement of the CSCs located in the forward small wheels of the muon spectrometer and adding new layers for the tracking performance improvement. A new design for the read-out electronics including triggering capabilities is also under consideration. Additionally, Phase I foresees an upgrade of the Forward Calorimeter, due to the possible beam heating

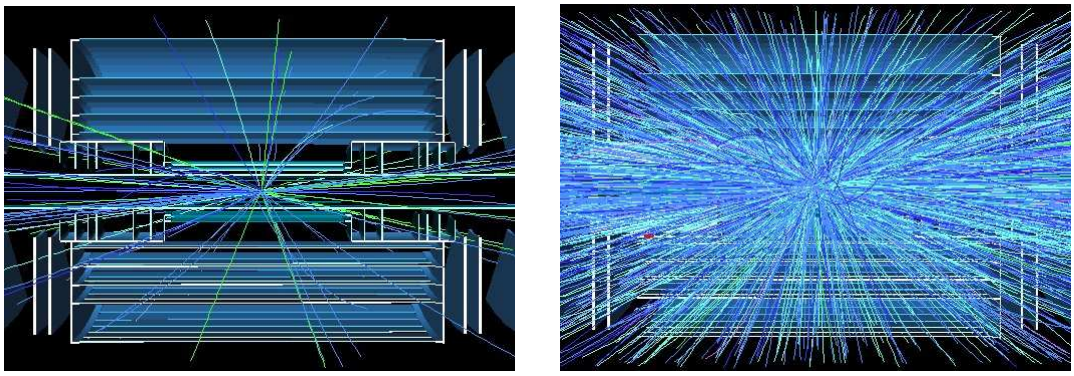

Figure 1.5: Simulation of the particle tracks resulting from the proton-proton collisions corresponding to the luminosity of $0.2 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ (left) and $10 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ (right) [43].

of the liquid argon and radiation effects in the front-end electronics. Several solutions are under investigation, including the installation of a warm FCal in front of the existing Forward Calorimeter [44] using diamond detectors or high pressure Xenon ionisation chambers. Another idea is to replace the FCal with so-called Mini-FCal, having smaller gaps, new summing boards and additional cooling.

Phase II of the upgrade assumes replacement of the Inner Detector and further changes in the forward region of the Muon Spectrometer, including the replacement of the Monitored Drift Tubes and Cathode Strip Chambers installed during Phase I. The radius of MDTs is planned be reduced from 30 mm to 15 mm in order to decrease the space charge in the detector. There are also many R&D studies ongoing, including the development of Micromegas[4] or Gas Electron Multiplier[5], aiming at the upgrade of the forward trigger system.

1.3.4 Upgrade of the Inner Detector

A project called the Insertable *B*-Layer (IBL) [46] has recently been accepted for the Pixel Detector upgrade in Phase I. It assumes adding an extra layer of pixel sensors into the tracker, very close to a new berillium beam pipe. After Phase I, the Pixel Detector, together with the IBL, will cover a range in pseudorapidity of $|\eta| \leq 3.0$. Although the installation of the beam pipe and new B-layer is a very non-trivial engineering operation, it should significantly improve the space resolution, which will have a great impact on the

[4]MicroMEsh GAseous Structure (Micromegas) – a double stage parallel plate avalanche counter developed at CERN for high energy physics application [45].

[5]Gas Electron Multiplier (GEM) – another gaseous detector developed originally at CERN, consisting of thin polymer foil(s), metal coated on both sides and chemically etched holes of high density [45].

physics analyses.

New pixel sensors located 31 mm from the interaction point will have to survive several years in a harsh environment, where the 1 MeV neutron equivalent fluence is estimated to be around $5 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ [47]. After intensive studies two different sensor technologies were chosen to be used in the IBL, namely slim edge silicon *n*-in-*n* type planar sensors and 3D sensors etched in a *p*-type substrate.

The ATLAS Inner Detector was designed for integrated luminosity of around $740\,\mathrm{fb}^{-1}$ [48]. Thus, the radiation damage is not an issue for the current tracker, since the integrated luminosity accumulated until 2020 should be around $320\,\mathrm{fb}^{-1}$ [40]. However the integrated luminosity accumulated in 5 years of the HL-LHC operating with nominal luminosity of $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ will exceed $3000\,\mathrm{fb}^{-1}$ and the estimated fluence of 1 MeV neutron equivalent in the innermost (*B*-layer) will be around $2 \cdot 10^{16}\,\mathrm{n_{eq}/cm^2}$ [49]. The profile of the 1 MeV neutron equivalent fluence as a function of the distance from the beam pipe after Phase II is shown in Fig. 1.6.

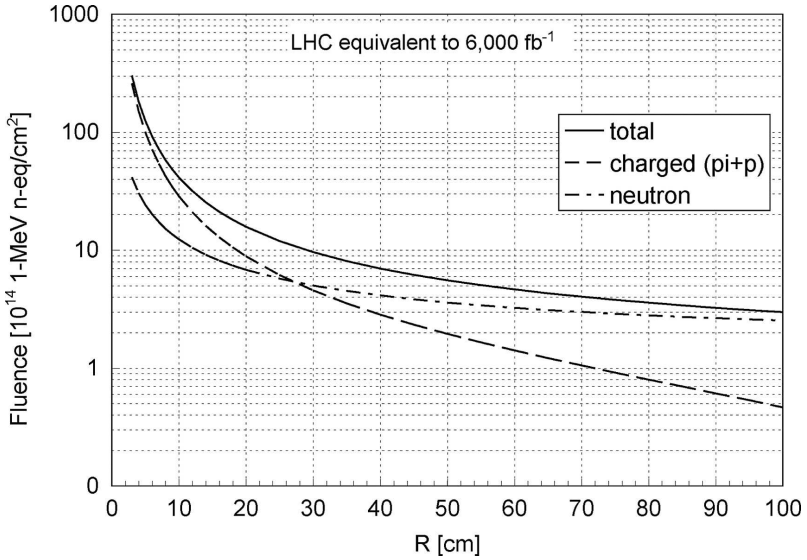

Figure 1.6: 1 MeV neutron equivalent fluence in the ATLAS Inner Detector after the Phase II of the High Luminosity Upgrade as a function of the radial distance from the beam axis (simulated for the luminosity of $6000\,\mathrm{fb}^{-1}$, including the safety factor of two with respect to the expected sLHC luminosity) [49].

The requirements for radiation hardness and high detector granularity lead to the ultimate solution, the replacement of the Inner Detector in Phase II. A new ID must be designed in a way that guarantees good tracking capabilities at high collision rate. The new detector must also meet strict requirements related to power dissipation and material budget limits. It will be an all-silicon detector, using pixel detector technology at small

radii and silicon strip technology at mid and large radius layers. The removal of the Transition Radiation Tracker is required. A layout proposed for the new ATLAS tracker is shown in Fig. 1.7.

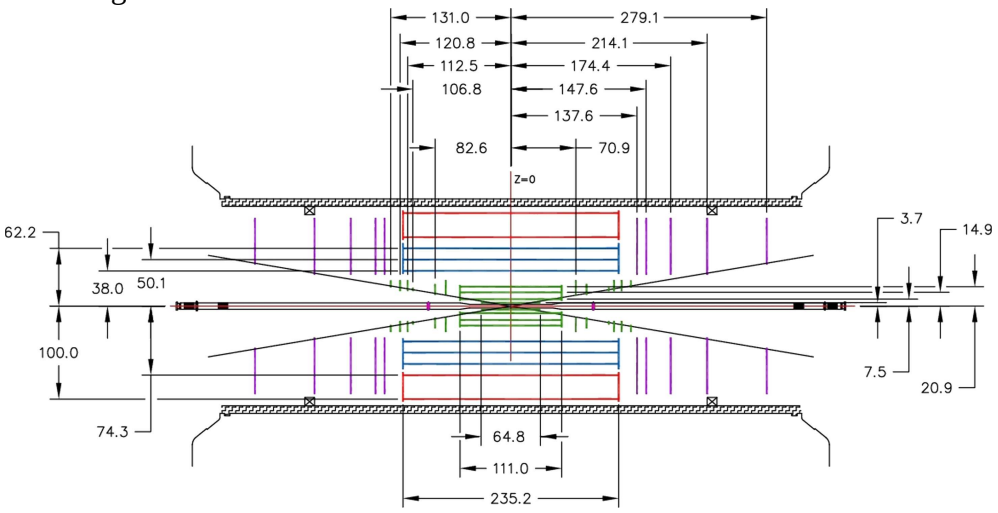

Figure 1.7: Layout proposed for the ATLAS Inner Detector after the Phase II of the High Luminosity Upgrade; pixel layers (green), short strips (blue), long strips (red) [50].

The detailed architecture of the new Pixel Detector is still under investigation, however most probably it will be organised into four concentric barrel layers and six disk layers in each end-cap region, providing $160 \cdot 10^6$ read-out channels. The area covered by the pixel sensors will be around $3.2\,\mathrm{m}^2$, so almost two times larger than it is today. One of the considered solution [51] assumes the innermost layer of pixel tracker being manufactured in new, extremely radiation hard, but expensive technology (diamond sensors or Full-3D silicon sensors with active edges), while the outer layers would be designed in cost-efficient, radiation hard n^+-in-n planar sensors.

The new Semiconductor Tracker considered for Phase II will comprise five layers of silicon strip detectors in the barrel region and five end-cap discs on each side, covering the total area of around $160\,\mathrm{m}^2$. The first barrel layer will be located at the radius of 38 cm from the beam, and the last one in the distance of 95 cm, covering the space occupied before by the Transition Radiation Tracker. In order to minimise the detector occupancy two different sensor strip lengths are considered. Three inner layers in the barrel region will be equipped in short strip sensors, 2.4 cm long with 75 μm pitch. For the remaining two outer layer sensors having longer strips of 9.6 cm are planned [48]. The total number of the read-out channels planned for the strip detector is almost $42 \cdot 10^6$.

The design of the SCT end-cap regions seems to be more complicated. In the forward region the sensors will be organised in 10 double-sided discs (5 discs on each end-cap

side). Each disc will then comprise 32 identical petals (except the last disc on each side, which drops the inner ring modules) assuring the radial coverage between 336 mm and 951 mm and coverage in z between 1376 mm and 2791 mm [52]. The end-cap sensors will most probably need 6 different shapes of silicon sensors. Two different lengths of the silicon sensors are considered, short strips of around 25 mm and medium strips of around 50 mm.

The higher granularity of the detector will provide good track reconstruction. The shorter silicon strip sensors, comparing to the ones currently used, will also result in lower detector capacitance and hence will improve the Equivalent Noise Charge. A simplified formula for the ENC is shown in Eq. 1.4 [53]:

$$ENC \equiv Q_N = \sqrt{a_n \tau + b_n \frac{C_i^2}{\tau} + 4A_f C_i^2}, \tag{1.4}$$

where a_n and b_n are the spectral noise densities of the parallel and series noise sources at the input of the front-end circuit, C_i is the total capacitance shunting the input, τ is the peaking time of the shaper and A_f is the $1/f$ noise coefficient.

One can immediately note that the ENC is strongly dependent on the capacitance C_i, so also the detector capacitance. Additionally, the parameter a_n in Eq. 1.4 is proportional to the detector current including the dark (leakage) current. Since the dark current increases after irradiation and is proportional to the sensor area, also in this aspect the small sensors have advantage over the big ones.

The silicon strip sensors planned to be used in the new Semiconductor Tracker will most probably be manufactured in radiation hard, planar *n*-in-*p* technology, which according to the recent studies and prototype tests will meet all the requirements [54]. The use of *n*-in-*p* silicon sensor technology is in this case fully justified, because the signal generated by a particle traversing the *n*-in-*p* sensor is dominated by electrons, not holes. Electrons are also less affected by trapping at defects induced by radiation [49]. The *n*-in-*p* sensors do not undergo type inversion [55], as is case for the *p*-in-*n* sensors used in the current tracker, and thus they can operate properly after being irradiated up to high doses. This capability is especially important considering the fact that the inner layers of short strips will have to withstand the NIEL of $6.0 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$ and TID of 262 kGy. For the outer SCT layers, NIEL will be two times lower, around $2.8 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$, while TID should be around 79 kGy[6].

[6] 1 MeV neutron equivalent fluence and the Total Ionizing Dose in silicon strip detectors calculated for the integrated luminosity of $3000\,\mathrm{fb}^{-1}$.

Power distribution system in Semiconductor Tracker after the High Luminosity Upgrade

The selection of the power management scheme for the future SCT is one of the most important issues and is currently the subject of advanced R&D studies. One should note that the increase in the detector granularity will seriously affect the power consumption in new the Inner Detector. Although the power consumption in a single channel is expected to be reduced significantly, the supply current will be reduced to a lesser degree and thus delivering power to the front-end chip will become a big issue.

Currently, the SCT is comprised of 4,088 modules and each of them is powered independently. This means 4,088 cable chains distributing analogue and digital power, needed for the optical read-out system, clock and control links, and the sensor bias voltage. The power cables are of the order of 100 m long and this leads to the cable resistance of a few ohms. It was measured that 50 % – 80 % of the power from the power supplies is dissipated in the cables [56] through resistive heating.

The scheme assuming a single detector module being supplied with a separate cable set will be prohibited in the future SCT. There are two main reasons. Firstly, the increase of the read-out channels would require new cables. Their number, available for the future Inner Detector, is however limited by the number of cables currently placed inside the ATLAS. No new cables can be added because of the lack of space in the region of the cryostat and the calorimeters. Secondly, adding the new cables would have a considerable influence on the material budget. It has been calculated that if the individual powering scheme was implemented in the SCT after the High Luminosity Upgrade, the material budget would have been increased up to unacceptable level of 3 % of radiation length (X_0) [56].

Impact of the material budget on the tracking performance

The material budget in the current Inner Detector regarding the contribution to the radiation length of ID sub-detectors and different ID components is shown in Fig. 1.8. One can see that the contribution of cables and services to the material budget is not negligible.

The precision of the tracking system is described by the impact parameter resolution – σ_{d_0}. There are two components limiting σ_{d_0}, namely the finite point resolution of the detector and the uncertainty in the track measurement due to the multiple Coulomb scattering in the beam pipe and the tracker material. The impact parameter resolution is

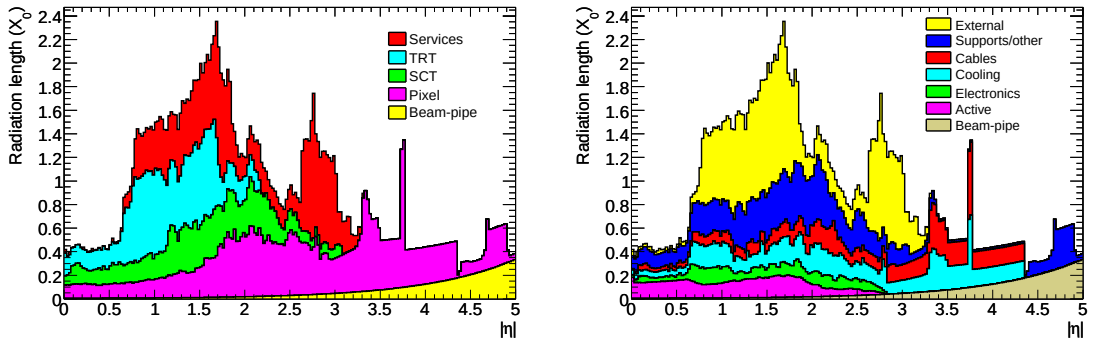

Figure 1.8: Material distribution in current Inner Detector as a function of $|\eta|$ averaged over ϕ. The contribution of external services and individual sub-detectors (left) and the contribution of different detector components (right) [23].

given by the following formula [57]:

$$\sigma_{d_0}^2 = a^2 + \frac{b^2}{p^2 \sin^3\theta}, \tag{1.5}$$

where p is the momentum of the particle and θ is the polar angle. The first term of Eq. 1.5 gives the intrinsic resolution of the detector itself, while the second is the component responsible for the multiple Coulomb scattering. The actual dependence between the full impact parameter resolution and the material budget is hidden in parameter b, which according to [58] is equal to:

$$b = 13.6\,\text{MeV} \cdot r_1 \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \cdot \ln\left(\frac{x}{\sin\theta \cdot X_0}\right)\right]. \tag{1.6}$$

The parameter x/X_0 is the material thickness, expressed in the radiation lengths, while r_1 is the distance between the vertex and the scattering medium, e.g. the beam pipe. The Equations 1.5 and 1.6 show that while increasing the amount of material within the detector volume one increases the parameter b and degrade the tracking performance of the detector.

Estimate of the power consumption in the SCT after High Luminosity Upgrade

A precise estimation of the power budget in the new SCT is a key element in the new tracker design process. The amount of power delivered to the detector and the amount of power lost inside its volume will have an impact on the architecture of the power distribution scheme, cooling system, et cetera. Despite the fact that many simulations in

this area have already been made, some of the numbers presented in this paragraph are still based on rough estimations [59]. Even the results obtained from the measurements of ABCN-25[7] cannot give all the answers about the power consumption in the ultimate design, simply because the final version of the chip will be designed using a different technology.

The final 256-channel front-end chip, ABCN-13, will be fabricated in 0.13 μm CMOS technology. The current consumption in the analogue electronics of a single read-out channel is estimated to be around 250 μA. It means that 256 analogue read-out channels will have to be fed with 64 mA. The amount of current consumed in the digital part has been estimated on the basis of results obtained from ABCN-25 and is around 105 mA.

Assuming the analogue supply voltage of $V_{ana} = 1.2\,\mathrm{V}$ and digital of $V_{dig} = 0.9\,\mathrm{V}$, the power consumption in analogue and digital part of ABCN-13 will be around 77 mW and 95 mW, respectively. Hence, the power consumption in a single read-out chip is around 170 mW.

One should note that the upgraded SCT, similarly to the present tracker, will have a highly modular construction. The hybrid will be the basic building block, containing five read-out chips with 1,280 channels. Two hybrids will form a detector module, with 2,560 read-out channels. Finally, 12 modules will form an SCT barrel stave.

The overall power budget in the SCT is not complete without taking into account the control circuitry and optoelectronics located on the hybrids and on each stave. Naturally, the major part of power delivered to the stave will be consumed in the front-end electronics (240 read-out ASICs), but one should not forget about power dissipation in the Hybrid Controller Chips (HCC), optoelectronics, slow control circuitry and especially in the Stave Controller Chip (SCC). The supply voltage, required current and power consumption of the SCT stave components are summarised in Table 1.2.

Based on these numbers, one can calculate the power consumption of a single detector hybrid and a stave. The hybrid consists of five 256-channel ABCN-13 chips and the HCC, thus it will consume approximately 1.04 W of power. The stave consists of 24 hybrids, the control electronics (SCC with slow control) and optoelectronics. This gives a total power consumption of approximately 27 W for $30.72 \cdot 10^3$ silicon strips.

[7] The first generation of the read-out chip for the future ATLAS SCT designed and manufactured in 0.25 μm CMOS technology.

Table 1.2: Power consumption in different SCT stave components.

	Supply voltage [V]	Current consumption [mA]	Power dissipation [mW]
Analogue electronics	1.2	64	77
Digital electronics	0.9	105	95
Hybrid Controller Chip	0.9	200	180
Stave Controller Board:			
– Optoelectronics	2.5	200	500
– Stave Controller	1.2	1080	1296
– Slow Control	1.2	50	75

Power efficiency of the power distribution system

The overall power efficiency of the power distribution system (η_S) can be defined as [56]:

$$\eta_S = \frac{1}{1 + I_m R_c / V_{DD}}, \tag{1.7}$$

where I_m is a module current, V_{DD} is the supply voltage and R_c is a resistance of a cable delivering power to the front-end electronics. The overall power efficiency in the current SCT was calculated to be slightly above 50 %, assuming the cable resistance of 4.5 Ω, the module current of 1.5 A and supply voltage in analogue and digital circuitry of 3.5 V and 4.0 V, respectively. Further decrease of the supply voltage and the increase of the detector granularity in the future will affect the efficiency, which can go down to around 10 % (assuming $R_c = 4.5\,\Omega$, $V_{DD} = 1.2$ V and $I_m = 2$ A, estimated for the SCT upgrade).

In order to keep reasonably high power efficiency and low material budget at the same time, a new powering scheme for the upgraded ATLAS SCT must be investigated. There are two completely different solutions for the system delivering power, currently under development:

- serial powering of several modules on a stave,
- powering of detector modules from a high voltage source with DC-DC converters.

The discussion presented above, together with the numbers summarised in Table 1.2 becomes a starting point in development of the CMOS integrated circuits (i.e. switched capacitor DC-DC converters and linear voltage regulators) for the power distribution system in the upgraded SCT, which is the main aim of this thesis.

Serial powering concept

In the serial powering scheme the chain of serially connected modules is supplied from a current source. The supply voltage for each module in the chain will be provided by a local shunt regulator. Thanks to this solution, one can significantly reduce the amount of power dissipated inside the detector volume, because the resistive power losses are given by $nI_{\mathrm{m}}^2 R_{\mathrm{c}}$, where n is the number of detector modules. Thus, when supplying 24 modules with one cable set, the power losses can be decreased by the same factor. This is true while assuming no power losses in the regulators. In the real case, power will be lost in shunt and linear regulators, and DC-DC converters. Another major advantage of the serial powering scheme is that the space occupied by the cables inside the tracker will not be increased, keeping the ID material budget unchanged.

Currently, three complementary approaches of the SCT serial powering scheme are being considered by the ATLAS collaboration. Each implementation, briefly described below, differs on the actual location of the shunt regulator and the power transistor. The proposed solutions are also presented in the Fig. 1.9.

1. One shunt regulator and one shunt transistor on a module is the simplest configuration. However it requires a separate power chip mounted on a module. Additionally a power transistor regulating supply voltage would have to be able to carry a whole module current in case of a failure condition.

2. Shunt regulator and shunt transistor on each read-out ASIC allows avoiding the situation, when the module current has to be sunk by one power device. The dedicated, external power chip is not needed, either. The main disadvantage of this configuration is related with the matching issues and switch-on conditions. The situation, when one power transistor draws most of the module current is possible and potentially destructive.

3. One shunt regulator on a module and shunt transistor on each read-out ASIC avoids shunt regulators mounted in parallel, however resistance and inductance of the bond wires, as well as the hybrid power traces / planes might have an influence on the circuitry performance at high frequencies.

One should note that each front-end ASIC consists of analogue and digital circuitry, located inside two separate power domains. In fact, an additional, third power domain for the optoelectronics circuitry on the module is required. The analogue supply voltage (V_{ana}) will be set to 1.2 V, but the exact value of the digital supply voltage (V_{dig}) is still under discussion. Most of the digital domain will be supplied with 0.9 V, however

an option of $V_{dig} = 1.2\,V$ is considered as well. The two basic configurations currently considered for the voltage distribution between the power domains are shown in Fig. 1.10.

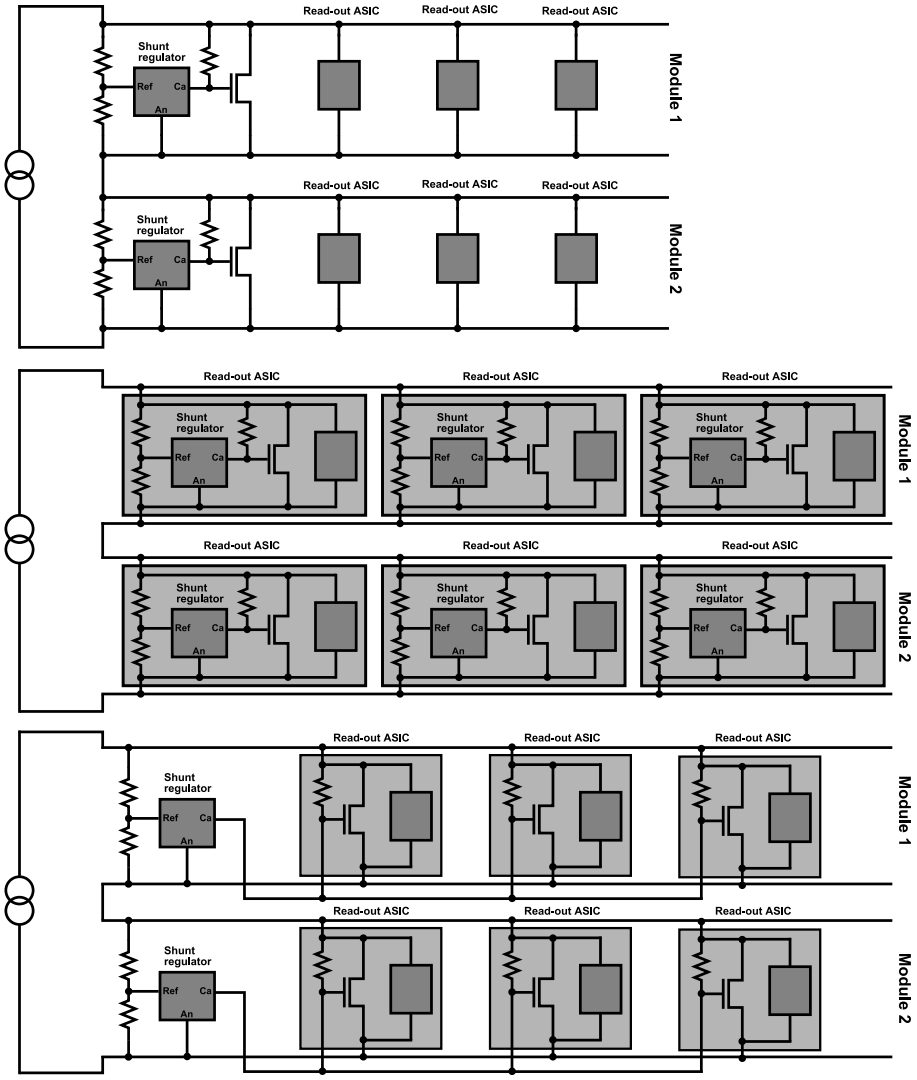

Figure 1.9: Possible implementations of the serial powering scheme; option with a dedicated powering chip on a hybrid (top), option with shunt regulator and shunt transistor mounted on each read-out chip (middle), option with one shunt regulators and shunt transistors mounted on each read-out ASIC (bottom).

The first implementation, presented in Fig. 1.10a, assumes that the analogue supply voltage, $V_{ana} = 1.2\,V$, is provided directly by a shunt regulator. In order to supply the digital circuitry, the analogue voltage is then lowered by a local LDO voltage regulator to $V_{dig} = 0.9\,V$. This option guarantees reasonable efficiency, approximately 69 % [60], however the quality of the analogue supply voltage is not very high.

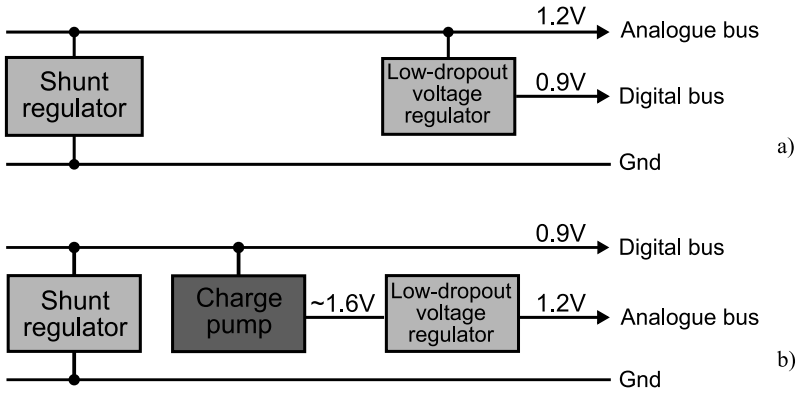

Figure 1.10: Internal analogue and digital supply voltage generation options foreseen for the use in serial powering scheme.

In the second case, shown in Fig. 1.10b, the digital circuitry is powered directly from a shunt regulator. In order to obtain higher analogue voltage a charge pump (step-up switched capacitor DC-DC converter) is needed. The output voltage from the converter can then be lowered and filtered by a linear voltage regulator to provide clean supply voltage of 1.2 V for the analogue circuitry. This solution allows for good quality analogue and digital voltage, thanks to low output impedance of the shunt regulator and good filtering efficiency of the linear regulator.

Most recent studies have shown that supplying the digital circuitry with 0.9 V might not be the optimal solution, for at least three reasons. Firstly, the sensitivity to Single-Event Upsets (SEUs) is highly dependent on the supply voltage, the higher the supply voltage the lower the SEU cross-section [61]. Secondly, the digital standard cells have not been parametrised for the supply voltage of 0.9 V. Thirdly, the performance degradation due to the Total Ionizing Dose caused by radiation is unavoidable and higher supply voltage will increase the electronics' tolerance to TID.

DC-DC conversion scheme

The idea of powering detector modules using a DC-DC conversion technique is more conventional than the serial powering solution, presented above. More accurately, in the DC-DC powering scheme the losses are given by $n(I_{\mathrm{m}}/g)^2 R_{\mathrm{c}}$, where g is the conversion factor of the power converter. In order to make DC-DC scheme competitive with the serial powering scheme in terms of power efficiency, the conversion factor must be kept sufficiently high. This can be obtained relatively easy by incorporating two power conversion stages. The basic principle of the scheme using separate step-down DC-DC converters is shown in Fig. 1.11 [62].

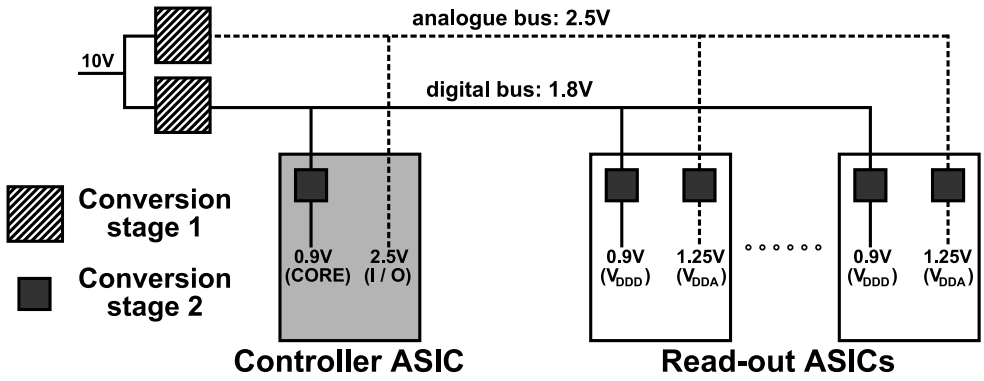

Figure 1.11: DC-DC powering distribution scheme supplied with 10 V, providing separate analogue and digital power domains.

The ATLAS SCT stave will be supplied with 10 V. The circuitry of the first conversion stage, located on a stave or a hybrid, will then provide two intermediate bus voltages: 2.5 V for analogue / optoelectronics and 1.8 V for digital. These voltages will be distributed along the stave supplying the front-end chips. A second power conversion stage, integrated into each front-end chip, will divide the voltages again, this time by a factor of two. Hence, the overall conversion ratio will be around 10. The above description of the DC-DC scheme does not assume any power losses in the converters.

The first conversion stage will consist of two buck converters characterised with the power conversion factors of $g = 4$ and around $g = 5.5$. A buck converter is a simple and robust solution which allows reaching high power efficiency, i.e. between 80 % and 85 % for the nominal current. The technology used in the design process must fulfil two main requirements: to be able to work with voltages up to 10 V with some safety margin and to guarantee full integration with the control circuit on an ASIC. The first buck converter prototypes, planned to be used in first stage, were fabricated in 0.35 µm technology, but several other commercially available technologies are currently under investigation as well. Nevertheless, the use of buck converters also brings some problems which have to be solved. Namely, all commercially available buck converters are designed to work with ferromagnetic inductors. These inductors guarantee high inductance, but they are not suitable for operation in high magnetic fields and saturate in $2-4$ T. Thus, there is a need to provide custom, high radiation tolerant buck converters using air-core inductors.

The second stage of the DC-DC power distribution scheme will contain two step-down switched capacitor DC-DC converters, located directly on the read-out chip. The converters will be used as dividers by 2, in order to provide the final supply voltages for the analogue and digital domain (1.2 V and 0.9 V). Converters of the second stage

will have to carry intermediate levels of current, of a few tens up to one hundred milliamperes. Switched capacitor converters are planned to be used here, because incorporating inductors is not possible in the second conversion stage.

In conclusion, the implementation of the DC-DC powering scheme is a challenging task, because of two reasons. Firstly, both conversion stages will be operating in a high radiation field. Surely this will have an influence on the performance of the converters and will downgrade the key parameter – the power efficiency. Thus, the circuits must be designed in radiation hard technology with all the necessary precautions. More detailed characterisation of the state-of-the-art 130 nm CMOS RF technology planned for switched capacitor converters design will be described and discussed in the next chapter. Secondly, the buck converters will have to employ air-core inductors for storing energy, to withstand a high magnetic field. This will seriously affect the material budget in the Inner Detector. On the other hand the DC-DC powering scheme guarantees high modularity, which allows turning off individual modules in case of failure. It also does not require the load currents to be constant in time.

Power building blocks presented in this thesis

Three different building blocks, intended to be implemented in the future SCT powering schemes are discussed in the following chapters of this dissertation. The serial powering scheme assumes the use of a switched capacitor DC-DC step-up converter and a linear voltage regulator, while the powering scheme based on the DC-DC conversion technique will employ a switched capacitor DC-DC step down converter. All presented prototype blocks were designed and fabricated in the IBM 130 nm CMOS technology.

The switched capacitor DC-DC converters are discussed in Chapter 3, while the two architectures, a classical voltage regulator employing an NMOS transistor and an LDO voltage regulator using a PMOS transistor as a pass device, are presented in Chapter 4.

Chapter 2

Radiation tolerance of deep submicron technologies

The modern CMOS technologies are becoming intrinsically radiation tolerant due to the thinner silicon dioxide in the transistor gates. The technology currently considered as a main candidate for the electronics upgrade is the IBM CMOS process with a lithography node of 130 nm, using 350 nm deep Shallow Trench Isolation (STI).

In order to characterise the radiation tolerance of the technology, numerous tests of semiconductor structures containing tens of different semiconductor devices were performed. This chapter consists of a brief overview of the radiation induced damage in the semiconductor structures, the description of two different CMOS technologies (90 nm and 130 nm), together with the results obtained from the irradiation tests.

2.1 Overview of the radiation induced damage in the semiconductor devices

Semiconductor devices exposed to radiation can be affected by three types of radiation damage mechanisms, namely displacement damage, ionisation damage and Single-Event Effects (SEEs).

Displacement damage occurs when radiation, heavy particles or neutrons, displace atoms in the cristalline lattice from their original positions, creating point defects and defect complexes in a semiconductor material. Defects created by radiation reduce the minority charge lifetime. One should note that the lifetime of the minority carriers does not significantly affect the operation of MOS transistors, but the effect is significant in bipolar devices [63] and leads to the degradation of the DC gain at low currents.

Nevertheless, an increase of the leakage current due to displacement damage can also be observed in MOS devices.

Displacement damage is proportional to the non-ionising energy loss, which depends on the type of the particle and its energy [64]. It manifests itself in three main possible ways:

- create mid-gap states that allow for the electron transition from the valence band to the conduction band, leading e.g. to the increase of current in the reverse biased *pn* junctions;
- create states located close to the edges of the band that can capture charge and release it after some time (trapping); and
- change the effective doping concentration.

The radiation damage caused by ionising radiation is much more serious in MOS technologies than the damage occurring due to displacements in the cristalline lattice. Photons with energies higher than the bandgap (1.1 eV for silicon and 9 eV for silicon dioxide), electrons, protons and ions can all be sources of damage [65]. Ionising radiation leads to the creation of the electron-hole pairs in the substrate and silicon dioxide, as well as the breaking of atomic bonds. This results in the degradation of the transistor performance. The MOS devices experience the following phenomena: a threshold voltage shift; increase of the leakage current; and decrease of the transistor gain.

A term Single-Event Effect covers a very wide spectrum of radiation effects caused by charge deposited by a single ionising particle. Among these effects one can enumerate: single-event upset (SEU), single-event transient, single-event latch-up, single-event gate rupture, and others. The sensitivity to the SEEs increases with the MOSFET size and the circuit speed [66].

2.1.1 Physical basis of the total ionising dose radiation effects

The main source of the total ionising dose radiation damage in the CMOS devices is located in the silicon dioxide. Hence, the key to understanding the total ionising dose radiation effects in the semiconductor devices is to understand the processes occurring in the gate oxide. There are three effects that lead to the occurrence of these types of radiation effects in MOS structures:

- a buildup of trapped charge in the silicon dioxide;
- an increase in the number of bulk oxide traps; and

- an increase of the interface traps close to the surface between silicon and silicon dioxide.

It is important to remember that electron-hole pairs are created in MOS devices as an effect of interaction of the ionising radiation with both, the insulator (silicon dioxide) and the silicon substrate. The electron-hole pairs created in the silicon are mobile and can be transported either by drifting in the electric field or by diffusion [64]. The transported carriers can be seen as transient currents. They can affect the operation of the semiconductor device, however they have no long-term effects on the device characteristics.

The situation is quite different in the case of e-h pairs generated in the oxide. The electrons are still mobile and can easily move towards the positive electrode thanks to the electric field, but the holes move by a slow and complex hopping mechanism. As a result, holes become more susceptible to trapping in the gate oxide. The holes are trapped by defects and stay there depending on the trap energy level. When a positive voltage is applied, holes can however drift slowly towards the Si/SiO_2 interface, where they are trapped acting like donors or acceptors.

There is also another process that leads to the creation of interface traps. The ionising radiation interacts with the matter and breaks the chemical bonds in the SiO_2 structure. A fraction of the bonds may reform when the electrons and holes recombine, but the remaining ones can create electrically active defects. These defects can migrate towards the Si/SiO_2 interface and form interface traps. The broken chemical bonds associated with the hydrogen or hydroxyl ($-OH$) groups may release impurities which are mobile in the oxide. These impurities can migrate to the interface between the Si and SiO_2 and undergo a reaction resulting in the interface trap creation. More details on the process leading to the creation of the interface traps can be found in [65].

2.1.2 Threshold voltage shift

The threshold voltage of both types of MOS transistors, *n*- and *p*-channel, is affected by the charge trapped in the oxide and the Si/SiO_2 interface. This charge changes the *C*-*V* curve of the MOS capacitor formed by the gate and the channel, thus it causes also the threshold voltage shift. The mechanism that is behind it is rather simple. The positive charge trapped in the oxide must be compensated by a more negative voltage applied on a gate of the transistor. This results in a lower absolute value of the threshold voltage in *n*-channel transistors and a higher absolute value of the threshold voltage in *p*-channel devices. One should also note that the magnitude of these effects depends on several

factors, e.g. dose rate, bias conditions, temperature, etc.

As mentioned, the overall effect of the threshold voltage shift (ΔV_{th}) has two components, the first one related to the shift caused by the charge trapped within the oxide (ΔV_{ot}) and the second one related to the charge trapped in the Si/SiO_2 interface, ΔV_{it}. Hence, it can be written as:

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it}. \tag{2.1}$$

For the *n*-channel transistors the positive charge trapped in the oxide decreases the absolute value of V_{th}, while the contribution from the holes trapped close to the Si/SiO_2 interface, observed at high doses or after long irradiation periods increases the V_{th}. These two effects are subtractive and result in a characteristic rebound. In the case of the *p*-channel transistors, both components are additive and the threshold voltage shifts monotonically with the accumulated dose.

The total charge generated by the ionising radiation inside the silicon dioxide (Q_{ot}) is proportional to its thickness (t_{ox}), while the oxide capacitance (C_{ox}) is inversely proportional to the oxide thickness, hence the threshold voltage shift is proportional to oxide thickness squared, Eq. 2.2 [67].

$$\Delta V_{th} = -\frac{Q_{ot}}{C_{ox}} \propto t_{ox}^2 \tag{2.2}$$

This dependence is presented in Fig. 2.1. Although the vertical axis represents the flat-band voltage (V_{fb}) not the threshold voltage, one should remember that the shift of V_{fb} is equal to the shift of V_{th}.

According to Fig. 2.1 scaling down the technology increases its intrinsic tolerance to the Total Ionizing Dose effects. The observed threshold voltage shift becomes less and less significant in modern technologies. The threshold voltage shift is reduced further below the t_{ox}^2 rule for the technologies with oxide thickness below 10 nm due to positive charge recombination with electrons tunnelling from both the gate and the silicon substrate.

2.1.3 Leakage current

Despite the significant reduction in the gate oxide thickness, the STI that is used to electrically isolate the transistors and surrounds the active devices on the wafer remains relatively thick. In case of the technology nodes that are discussed in this chapter, the STI thickness is around two orders of magnitude higher than the gate oxide. The radiation

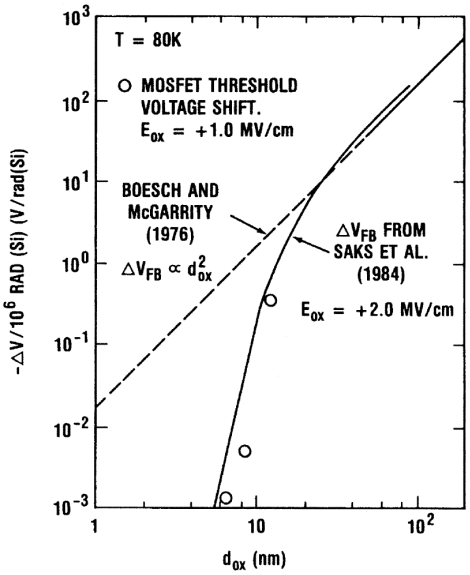

Figure 2.1: Flat-band voltage per unit dose as a function of the oxide thickness measured at 80 K [68]. Solid line represents the experimental points, while the dashed line corresponds to Eq. 2.2.

hardness of the semiconductor device becomes then strongly influenced by its geometry.

As it was explained in the previous paragraph, the silicon dioxide traps the positive charge inside its volume. This charge influences the value of the threshold voltage of a transistor. If the positive charge is big enough an inversion layer can be created close to the Si/SiO_2 surface. For a *p*-type substrate or a *p*-well the threshold voltage can be significantly reduced or even go below zero volts, hence an inversion layer may be induced underneath the STI. The inversion layer shorts the drain and the source of the NMOS transistor at the edge of the active region and causes a current flow. Figure 2.2 shows the layout and the cross section of a MOS transistor with possible leakage current paths.

Often, one can also observe an inter-device leakage. It is possible when the positive charge in the oxide creates the inversion layer between the adjacent *n*-channel transistors. Thus, the current flows between the drain of one transistor and source of another one.

In addition, in CMOS technologies using *n*-type doped wafers another possible path for the leakage current may exist. Due to the creation of the inversion layer underneath the STI a channel between the source of the transistor and the *n*-type substrate can be induced. However, this is not the case for the technologies described in this dissertation.

A commonly used method that allows for a significant reduction of the leakage current in an NMOS transistor is adopting the enclosed gate layout [69]. Three different layout approaches are shown in Fig. 2.3. The Enclosed Layout Transistors (ELTs) guarantee very low leakage current which does not change with the TID, but a designer must pay

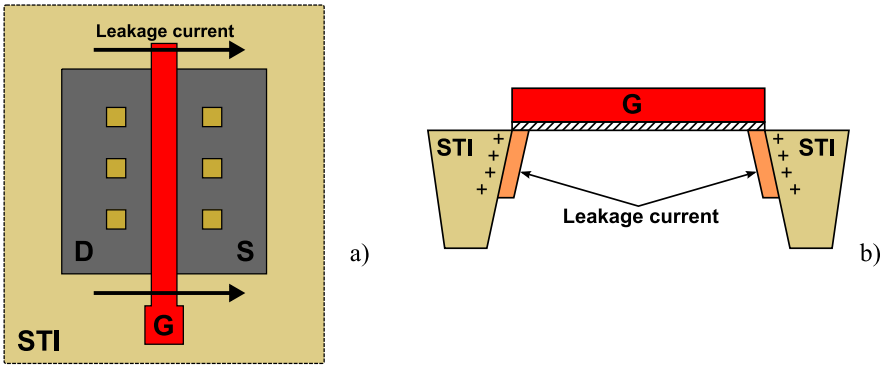

Figure 2.2: Layout of an NMOS transistor surrounded by the STI (a) and the cross section of the same transistor (b) with the current leakage paths.

a price in the higher transistor area. It has also been observed that the performance (in terms of speed, power consumption, etc.) of the circuits laid out with the ELTs may be different in comparison to a design laid out with the linear (two-edged-gate) transistors of the same W/L ratios.

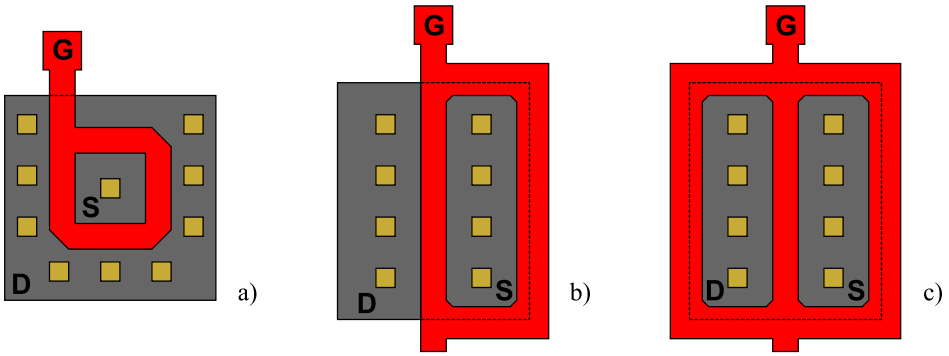

Figure 2.3: Layouts of NMOS transistors with enclosed gates; annular (a), ringed source (b), butterfly (c).

2.1.4 Change in subthreshold slope

The transfer characteristic of the MOS transistors changes significantly with the TID. Its simplified evolution is presented in Fig. 2.4, where the red curve represents the I_D-V_{GS} characteristic before irradiation and the blue curve – the characteristic of the same transistor after the irradiation.

For each MOS transistor operating in a weak inversion regime one can define a parameter called subthreshold slope (S) [70], which corresponds to a variation of the

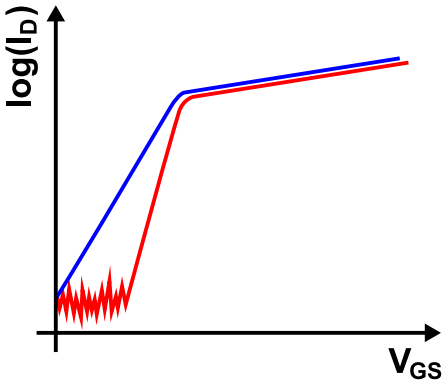

Figure 2.4: Transfer characteristic of a NMOS transistor before (red curve) and after the irradiation (blue curve).

gate-to-source voltage necessary for a ten-fold change of the drain current, as in Eq. 2.3.

$$S = \frac{\partial V_{GS}}{\partial (\log I_D)} = \ln 10 \left[1 + \frac{C_d + C_{it}}{C_{ox}} \right] U_T, \tag{2.3}$$

The depletion layer capacitance, the capacitance associated with the presence of the interface traps and the oxide capacitance are denoted by C_d, C_{it} and C_{ox}, respectively. The thermal voltage (U_T) is approximately 25 mV at room temperature

A typical value of S at room temperature is around 70 mV/decade. This means that the change of $\Delta V_{GS} = 70$ mV causes a ten-fold change in current value. One can note that the radiation induced increase in the interface trap density leads to the decrease of the subthreshold slope and thus the transistor becomes slower. In modern technologies, where the supply and the threshold voltage are scaled down, this effect becomes a serious issue, because it increases the leakage current [66].

2.1.5 Radiation induced mobility degradation

The carrier mobility degradation in a transistor channel is caused primarily due to charge trapped in the Si/SiO_2 interface, however a non-negligible contribution from the oxide trapped charge has also been reported [71]. The mobility is changed due to the Coulomb scattering from the charges induced by radiation. High reduction in the carrier mobility manifests itself as a decrease of the subthreshold slope, the transfer characteristics become less steep.

The expression describing the mobility degradation due to interface and oxide trapped

charge [66] is presented below:

$$\mu = \frac{\mu_0}{1 + \alpha_{it}\Delta N_{it} + \alpha_{ot}\Delta N_{ot}}, \tag{2.4}$$

where μ_0 is the pre-irradiation value of the carrier mobility, ΔN_{it} and ΔN_{ot} represent the density of interface and oxide trapped charge, respectively. Parameters α_{it} and α_{ot} quantify the influence of the interface traps and oxide trapped charge on mobility.

2.2 Tested CMOS technology nodes

This section consists of a brief overview of two deep submicron technologies, the CMOS9FLP/9RF 90 nm process and the CMOS8RF 130 nm process, for which radiation tolerance has been tested and is presented in the following paragraphs. One of these technology nodes, IBM CMOS 130 nm, has been used for the design of the switched capacitor DC-DC converters and the voltage regulators.

2.2.1 Overview of 90 nm 9FLP/9RF process

The CMOS9FLP process uses a moderately doped *p*-type substrate with a resistivity of $1-2\,\Omega$cm. The lithography node is 90 nm. The STI is nominally 0.43 µm deep into the silicon substrate. Depending on the version, a designer can choose between 6 and 9 levels of Cu metal and one Al level. The technology provides several types of transistors of both types, thin and thick gate oxide [72].

N-channel devices

Eight types of NFETs are available in the discussed 90 nm process. Apart from the regular-V_{th} n-channel devices, operating at the maximal voltage of 1.2 V, a designer can choose among several types of specific FETs, including super-high-V_{th}, high-V_{th}, low-V_{th} and zero-V_{th}. All mentioned transistors work with a maximum voltage of 1.2 V, with a nominal gate oxide thickness of 2.1 nm.

The thick gate oxide transistors are designed to operate with higher nominal voltages, namely 1.8 V, 2.5 V and 3.3 V. All three NFET types have the same gate oxide thickness of 5.2 nm.

The triple-well *n*-channel transistors can be used in both options, thin and thick gate oxide with almost all threshold voltage options (apart from the zero-V_{th}).

P-channel devices

The 90 nm 9FLP technology also supports several types of PFETs, namely super-high-V_{th}, high-V_{th}, regular-V_{th} and low-V_{th} devices also supplied with a maximum of 1.2 V. The gate oxide in case of these *p*-channel devices is thinner than for NFETs presented above, $t_{ox} = 1.9$ nm. High voltage devices are available in the following types: 1.8 V, 2.5 V and 3.3 V. All of them have thick gate oxides, $t_{ox} = 5.2$ nm.

2.2.2 Overview of 130 nm 8RF process

The CMOS8RF process is considered as the primary candidate for the SCT front-end electronics upgrade after the High Luminosity Upgrade of the ATLAS experiment. It uses *p*-type doped wafers with a resistivity of $1-2\,\Omega$cm. The lithography node is 130 nm. In order to provide proper isolation between the devices a CMOS8RF process uses shallow trench isolation (STI) which nominally is 0.35 µm deep into the silicon.

There are two options offered by the manufacturer, the "LM" and "DM". First of them uses five metal layers which results in lower manufacturing costs. The DM version provides additional low-resistivity metal layers suitable for the high quality RF components.

N-channel devices

The regular *n*-channel transistors offered with the discussed process are characterised for two operation voltages 1.2 V and 1.5 V. These are the thin gate oxide (core) devices in which the gate oxide thickness is 2.2 nm. Four variants of core NFETs are supported, namely high-V_{th} (low-power), regular-V_{th}, low-V_{th} and zero-V_{th}. Triple-well, thin gate oxide *n*-channel transistors are available as well.

There are two types of high voltage transistors, operating at 2.5 V or 3.3 V. They are optional thick gate oxide ($t_{ox} = 5.2$ nm) devices. They are available in all the voltage threshold variants, apart from zero-V_{th}. Triple-well, thick oxide NFETs are included in the technology.

P-channel devices

Complementary *p*-channel transistors are also available. Thin gate oxide PFETs ($t_{ox} = 2.2$ nm) are characterised for two operation voltages, 1.2 V and 1.5 V. They are available in three variants, depending on the threshold voltage, namely high-V_{th} (low-power), regular-V_{th} and low-V_{th}.

Thick gate oxide ($t_{ox} = 5.2\,\text{nm}$) can operate at 2.5 V or 3.3 V. They may be operated at up to 2.7 V and 3.6 V, respectively.

2.3 Test setup used for irradiation and measurement

A test setup used for the irradiation and measurement of these semiconductor structures is complex and consists of several elements, which are listed below:

1. an X-ray source (Seifert RP149);
2. a CCD digital camera used to monitor the alignment of the tested chip;
3. a probe card;
4. a thermal chuck used for chip positioning (Digit Concept DCT600);
5. a switching matrix mainframe (Keithley 707);
6. a semiconductor parameter analyser (HP 4145B);
7. an external power supply unit used for biasing under the irradiation (Agilent E3631); and
8. a PC running dedicated LabVIEW software.

The irradiation was performed using X-rays from the tube with Tungsten target, equipped with 0.25 mm thick Beryllium window. The tube was calibrated using a *p-i-n* diode. The maximum available tube current is 60 mA for a voltage of 50 kV. Figure 2.5 shows the irradiation cabinet with the X-ray generator used for the irradiation.

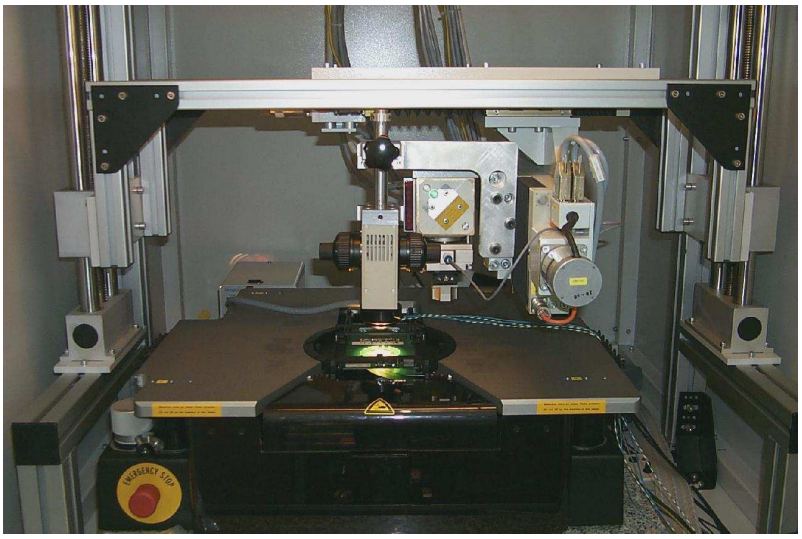

Figure 2.5: Cabinet with the X-ray generator used in the irradiation tests of the DCDC013 chip [73].

A remotely controlled thermal chuck allows keeping the chip at constant temperature during irradiation and measurements.

A probe card is an interface between the DUT and the switching matrix. The one used here contains two rows of 16 needles.

Each TID test structure contains over 20 different semiconductor devices, which should be efficiently irradiated and measured. The Keithley 707 switching matrix allows the user to pick a single device from the DUT and bias it accordingly to the need.

The HP 4145B parameter analyser is an instrument capable of complete high-speed DC characterisation of the semiconductor devices. The analyser contains four Source Monitoring Units (SMUs) which can be used as a voltage source / current monitor or current source / voltage monitor. Additionally, it provides two voltage measurement ports and two voltage sources. The value of each voltage or current source can be easily specified and the certain compliance limit can be set.

Agilent E3631 is a high accuracy and high resolution low noise power supply unit. It is used during the irradiation process to bias the semiconductor devices.

2.3.1 Semiconductor TID test structures

Two chips manufactured to evaluate the radiation tolerance of submicron CMOS technologies (130 nm and 90 nm) are presented in the following paragraphs. The chips were designed at CERN electronics group and are called TID3 and TID90, for 130 nm and 90 nm process, respectively. They consists of individual semiconductor devices: transistors, resistors and diodes that allow for monitoring of the degradation caused by radiation.

TID3 test chip

The TID3 test chip is a third generation of ASICs, designed to evaluate the radiation tolerance of the CMOS 130 nm technology. This technology node is meant to be a main candidate for the front-end electronics upgrade in the future ATLAS Inner Detector. The latest version of TID3, submitted in May 2010, has been tested and the obtained results are presented in this chapter. Its design has been significantly simplified, comparing to the previous versions, and contains only two blocks of semiconductor devices:

- block A with *p*-channel transistors, diodes, resistors and FOXFETs; and
- block B with *n*-channel transistors only.

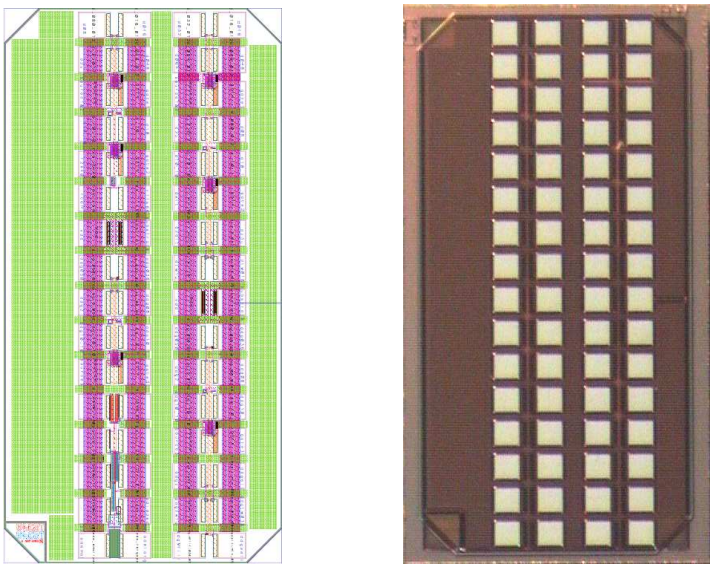

Figure 2.6: Layout of the TID3 from Cadence Virtuoso Layout Suite (left) and the microphotograph of the manufactured chip (right).

The layout and the microphotograph of TID3 are presented in Fig. 2.6. The 64 pads have been organised in 4 rows of 16 pads, allowing easy access for the probe needles. Due to the limited number of the needles only one block can be tested at one time.

The TID3 was designed to allow the evaluation of wide spectrum of radiation induced effects. Hence, it contains an array of minimum channel length transistors to investigate the radiation induced narrow channel effects and lateral leakage current phenomenon. An array of transistors with identical channel widths can be used to measure the dependence of the radiation effects on the channel length. The TID3 is also equipped with the ELTs.

A complete list of the transistors laid out in blocks A and B, their type and size, is presented in Tables 2.1 and 2.2.

TID90 test chip

The TID90 is equivalent to TID3 in the CMOS 90 nm process. It was submitted in 2009. The design of TID90 is however more complex than TID3, because the chip is divided into four separate blocks, A through D, containing:

- block A – an array of different types (regular-V_{th}, low-V_{th}) of *p*-channel transistors, FOXFETs, diodes and resistors;
- block B – an array of different types (regular-V_{th}, low-V_{th}, triple-well) of *n*-channel transistors;
- block C – an array of regular-V_{th}, *n*- and *p*-channel transistors with constant W/L

ratio of 12.5; and

- block D – an array of regular-V_{th} NFETs with constant W/L ration of 700.

Table 2.1: List of thin gate oxide transistors integrated on the TID3 test structure.

Thin gate oxide devices	
Transistor type	Transistor dimensions
- regular-V_{th} (NFETs and PFETs)	$W/L = 0.16\,\mu m/0.12\,\mu m$ $W/L = 0.32\,\mu m/0.12\,\mu m$ $W/L = 0.48\,\mu m/0.12\,\mu m$ $W/L = 0.64\,\mu m/0.12\,\mu m$ $W/L = 0.80\,\mu m/0.12\,\mu m$ $W/L = 2.00\,\mu m/0.12\,\mu m$ $W/L = 10.0\,\mu m/1.00\,\mu m$ $W/L = 10.0\,\mu m/10.0\,\mu m$
- regular-V_{th} ELT NFET	$W/L = 2.82\,\mu m/0.12\,\mu m$
- zero-V_{th} NFET	$W/L = 3.00\,\mu m/0.42\,\mu m$
- zero-V_{th} ELT NFET	$W/L = 3.35\,\mu m/0.42\,\mu m$
- regular-V_{th}, triple-well NFETs	$W/L = 0.16\,\mu m/0.12\,\mu m$ $W/L = 1.00\,\mu m/0.12\,\mu m$

Table 2.2: List of thick gate oxide transistors integrated on the TID3 test structure.

Thick gate oxide devices	
Transistor type	Transistor dimensions
- regular-V_{th} (NFETs and PFETs)	$W/L = 0.36\,\mu m/0.24\,\mu m$ $W/L = 0.50\,\mu m/0.24\,\mu m$ $W/L = 0.80\,\mu m/0.24\,\mu m$ $W/L = 2.00\,\mu m/0.24\,\mu m$
- regular-V_{th} ELT NFET	$W/L = 3.06\,\mu m/0.26\,\mu m$
- zero-V_{th} NFET	$W/L = 2.94\,\mu m/0.56\,\mu m$
- zero-V_{th} ELT NFET	$W/L = 3.74\,\mu m/0.56\,\mu m$
- regular-V_{th}, triple-well NFETs	$W/L = 0.36\,\mu m/0.24\,\mu m$ $W/L = 1.00\,\mu m/0.24\,\mu m$
- regular-V_{th} NFET with metal filling on top	$W/L = 0.36\,\mu m/0.24\,\mu m$

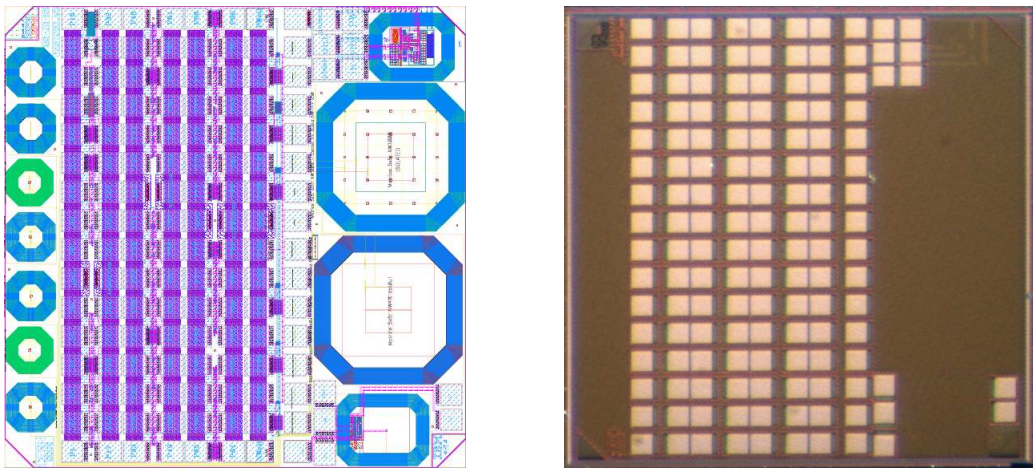

Figure 2.7: Layout of the TID90 from Cadence Virtuoso Layout Suite (left) and the microphotograph of the manufactured chip (right).

Similarly to the TID3 chip, also here each block has to be tested individually. The layout view and the microphotograph of the entire TID90 chip are shown in Fig. 2.7. It is equipped with 112 pads, divided into 7 rows of 16 pads.

This chapter contains results collected from the transistors laid out within blocks A and B, so only these blocks are considered here. The complete list of transistors, their types and sizes can be found in Tables 2.3 and 2.4.

Table 2.3: List of thin gate oxide transistors integrated on the TID90 test structure.

Thin gate oxide devices	
Transistor type	Transistor dimensions
- regular-V_{th} (NFETs and PFETs)	$W/L = 0.12\,\mu m/0.10\,\mu m$
- low-V_{th} (NFETs and PFETs)	$W/L = 0.24\,\mu m/0.10\,\mu m$
- triple-well (NFETs only)	$W/L = 10.0\,\mu m/0.10\,\mu m$
	$W/L = 10.0\,\mu m/1.00\,\mu m$
	$W/L = 10.0\,\mu m/10.0\,\mu m$
ELT NMOS transistor	$W/L = 2.78\,\mu m/0.10\,\mu m$

2.4 Measurement methodology

The results presented in this chapter come from the measurements carried out at CERN between 2009 and 2011. The test procedure applied to both chips (TID3 and TID90)

Table 2.4: List of thick gate oxide transistors integrated on the TID90 test structure.

Thick gate oxide devices	
Transistor type	Transistor dimensions
- regular-V_{th} (NFETs and PFETs)	$W/L = 0.36\,\mu m/0.24\,\mu m$
- triple-well (NFETs only)	$W/L = 0.72\,\mu m/0.24\,\mu m$
	$W/L = 2.00\,\mu m/0.10\,\mu m$
	$W/L = 10.0\,\mu m/1.00\,\mu m$
	$W/L = 10.0\,\mu m/10.0\,\mu m$
- ELT NMOS transistor	$W/L = 3.10\,\mu m/0.28\,\mu m$

is identical. First, the *I-V* curves of each transistor were accurately measured by the HP 4145. Then, a properly biased chip was irradiated up to a certain dose. The full test consisted of 13 – 15 steps, until the required TID was achieved. For instance, in order to reach the TID of 200 Mrad the chip had to be irradiated for about 80 hours. All the required parameters (threshold voltage, leakage current, transconductance, etc.) were extracted from the collected characteristics with dedicated MATLAB software. The following *I-V* curves were measured:

- a transfer characteristic, $I_D(V_{GS})$ for a given value of drain-to-source voltage (V_{DS}); and
- an output characteristic, $I_D(V_{DS})$ for a given value of gate-to-source voltage (V_{GS}).

Each measurement of a single transistor results in four *I-V* curves: two transfer characteristics and two output characteristics. In order to measure the transfer characteristics, the V_{GS} voltage was swept between $-0.2\,V$ and $1.5\,V$, for two fixed values of drain-to-source voltages, $V_{DS1} = 20\,mV$ and $V_{DS2} = V_{DD}$. Next, to measure the output characteristics the drain-to-source voltage was swept from zero to supply voltage, for two fixed values of V_{GS}.

Tables 2.5 and 2.6 contain the voltage ranges and the values of fixed voltages used by HP 4145 to measure the *I-V* curves of *n*-channel transistors on both chips. For the *p*-channel devices, the voltages of opposite polarity were applied.

2.4.1 Threshold voltage extraction procedure

Currently, each model used to describe the behaviour of a MOS transistor contains a large set of technological, electrical and adjusting parameters. One of the fundamental param-

Table 2.5: The voltage parametrisation of the NMOS transistors applied by the HP 4145 during the tests of 130 nm technology.

	130 nm technology node	
	thin gate oxide NFET	thick gate oxide NFET
Transfer characteristic	$V_{GS} \in [-0.2\,\mathrm{V}, 1.5\,\mathrm{V}]$	$V_{GS} \in [-0.2\,\mathrm{V}, 2.5\,\mathrm{V}]$
	$V_{DS1} = 0.02\,\mathrm{V}$, $V_{DS2} = 1.5\,\mathrm{V}$	$V_{DS1} = 0.02\,\mathrm{V}$, $V_{DS2} = 2.5\,\mathrm{V}$
Output characteristics	$V_{DS} \in [0.0\,\mathrm{V}, 1.5\,\mathrm{V}]$	$V_{DS} \in [0.0\,\mathrm{V}, 2.5\,\mathrm{V}]$
	$V_{GS1} = 1.0\,\mathrm{V}$, $V_{GS2} = 1.5\,\mathrm{V}$	$V_{GS1} = 1.5\,\mathrm{V}$, $V_{GS2} = 2.5\,\mathrm{V}$

Table 2.6: The voltage parametrisation of the NMOS transistors applied by the HP 4145 during the tests of 90 nm technology.

	90 nm technology node	
	thin gate oxide NFET	thick gate oxide NFET
Transfer characteristic	$V_{GS} \in [-0.2\,\mathrm{V}, 1.2\,\mathrm{V}]$	$V_{GS} \in [-0.2\,\mathrm{V}, 2.5\,\mathrm{V}]$
	$V_{DS1} = 0.02\,\mathrm{V}$, $V_{DS2} = 1.2\,\mathrm{V}$	$V_{DS1} = 0.02\,\mathrm{V}$, $V_{DS2} = 2.5\,\mathrm{V}$
Output characteristics	$V_{DS} \in [0.0\,\mathrm{V}, 1.2\,\mathrm{V}]$	$V_{DS} \in [0.0\,\mathrm{V}, 2.5\,\mathrm{V}]$
	$V_{GS1} = 0.8\,\mathrm{V}$, $V_{GS2} = 1.2\,\mathrm{V}$	$V_{GS1} = 1.5\,\mathrm{V}$, $V_{GS2} = 2.5\,\mathrm{V}$

eters is the threshold voltage. In the industry, during the technology characterisation, the value of V_{th} must be extracted very precisely, otherwise it can cause serious issues in the circuit operation. There are several methods [74] which allow the V_{th} extraction from the current-voltage characteristics of a transistor. Two of them were chosen for the data analysis:

- the constant current (CC) method; and
- the extrapolation in linear and saturation region method.

Constant current method

This method is widely used mainly due to its simplicity. The constant current method defines V_{th} as a gate-to-source voltage, corresponding to a certain, predefined and constant drain current I_D. This current is specified in the design manual and parameterised with the effective channel width W_{eff} and the effective channel length L_p. These parameters are defines as follows:

$$W_{eff} = W_{des} - \Delta W \tag{2.5}$$

and

$$L_p = L_{des} - \Delta L, \tag{2.6}$$

where W_{des} and L_{des} are the transistor's channel dimensions set by a designer, and ΔW and ΔL are the variations of channel width and length, respectively. These values are specified in the technology design manual [72], [75] for each type of available MOSFET.

The specific drain current is defined as:

$$|I_D| = 300\,\text{nA} \cdot W_{eff}/L_p, \tag{2.7}$$

for *n*-channel devices and:

$$|I_D| = 70\,\text{nA} \cdot W_{eff}/L_p, \tag{2.8}$$

for *p*-channel devices.

In order to extract the threshold voltage value from the transfer characteristic one has to calculate the value of the drain current according to the above formulas and find the corresponding gate-to-source voltage.

Extrapolation in the linear region method

The extrapolation in the linear region method is another simple and commonly used method of threshold voltage extraction. The MOS transistor is biased in the linear region if the following conditions are fulfilled:

$$V_{GS} \geq V_{th} \qquad \text{and} \qquad V_{DS} \leq (V_{GS} - V_{th})\,. \tag{2.9}$$

A general expression for the drain current, called the Sah equation, [76]:

$$I_D = \mu_0 C_{ox} \frac{W}{L} \left[V_{DS}\,(V_{GS} - V_{th}) - \frac{V_{DS}^2}{2} \right], \tag{2.10}$$

can be simplified to Eq. 2.11, assuming very low drain-to-source voltage.

$$I_D \approx \mu_0 C_{ox} \frac{W}{L} V_{DS}\,(V_{GS} - V_{th}) \tag{2.11}$$

The above equations predict that the drain current is a linear function of the gate-to-source voltage (V_{GS}) for a given drain-to-source voltage (V_{DS}). Hence, the threshold voltage can be found as an intercept of the tangent to the inflexion point of the I_D-V_{GS} characteristic with the V_{GS} axis. The inflexion point is found in a point where the transistor transconductance (g_m) reaches its maximal value [77]. The result of the V_{th}

linear extrapolation method is shown in Fig. 2.8.

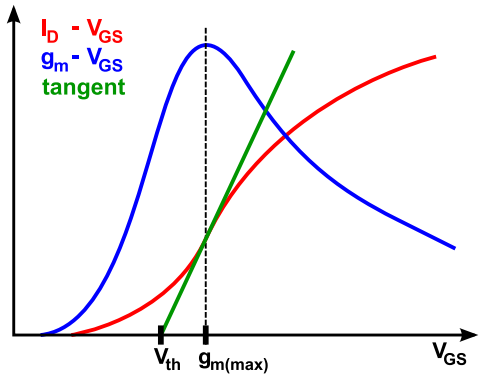

Figure 2.8: Threshold voltage extraction using the linear extrapolation method.

Extrapolation in the saturation region method

In the saturation region, where $V_{DS} > V_{GS} - V_{th}$, the drain current is described by a square law:

$$I_D = \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 . \tag{2.12}$$

By plotting the square root of the drain current $\sqrt{I_D}$ as a function of the gate-to-source voltage, one obtains a straight line [78]. From this point the procedure is identical to one presented in the previous case. The value of the threshold voltage is found at the point where the tangent to the inflexion point of the I_D-V_{GS} curve intersects with the V_{GS} axis.

2.4.2 Leakage current and on-current extraction procedure

Another crucial transistor parameter, for which evolution with the TID must be investigated is the leakage current. Its value can be extracted easily from the I_D-V_{GS} curve by measuring the transistor off-state drain current (I_{off}) at $V_{GS} = 0$. The I_{off} is influenced by many parameters [79], i.e. threshold voltage, channel physical dimensions, channel and surface doping profile, drain and source junction depth, and supply voltage.

Finally, the maximum saturation on-current (I_{on}) is a parameter that determines the circuit driving capability. This parameter can be extracted from both, transfer (measured in the saturation region) and output characteristic as the drain current (I_D) for the maximal value of the gate-to-source voltage.

2.5 Radiation tolerance of 130 nm CMRF8SF technology

This section contains the results collected from the TID3 test chip fabricated in 130 nm CMOS technology. Using an X-ray generator, block A of TID3, containing *p*-channel transistors was irradiated up to a TID of 100 Mrad, while block B, consisting of *n*-channel transistors, up to 200 Mrad.

2.5.1 Transfer characteristics

Figures 2.9 and 2.10 show two families of transfer characteristics measured for the thin oxide minimum size *n*- and *p*-channel transistor, respectively. According to the considerations presented in the introduction to this chapter, the TID is expected to have a greater impact on the leakage current in the *n*-channel transistor, than in the case of the *p*-channel device.

This is consistent with the measurements. A twenty-five fold change in the measured leakage current has been observed in an NFET ($W = 0.16\,\mu m$, $L = 0.12\,\mu m$), while in case of a PFET of the same size the observed change is roughly 2 times higher. Also a higher increase in the subthreshold swing is measured in the NMOS transistor.

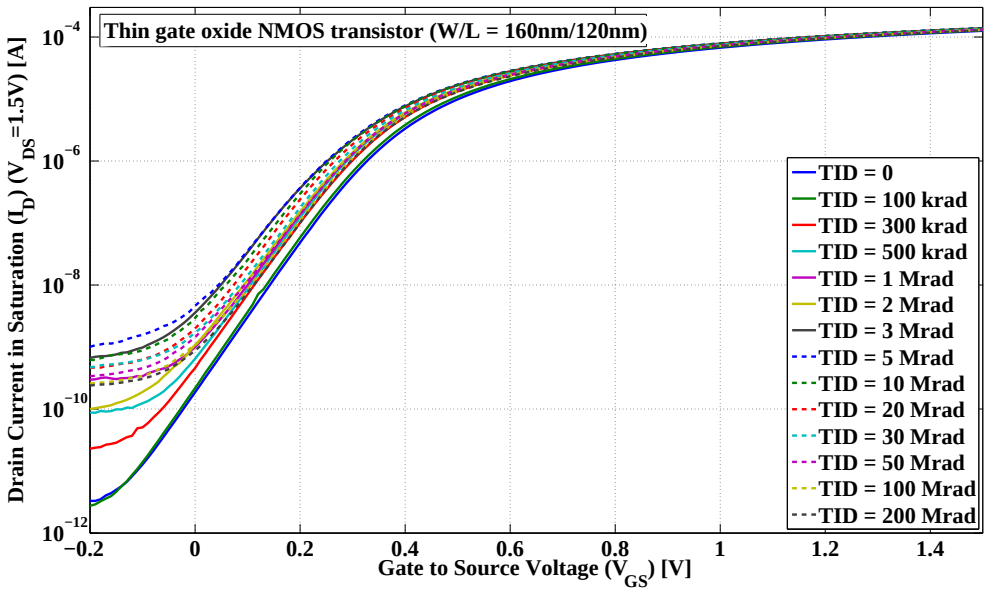

Figure 2.9: Evolution of the transfer characteristic with the TID for a minimum size ($W = 0.16\,\mu m$, $L = 0.12\,\mu m$), thin gate oxide, *n*-channel transistor manufactured in 130 nm technology node.

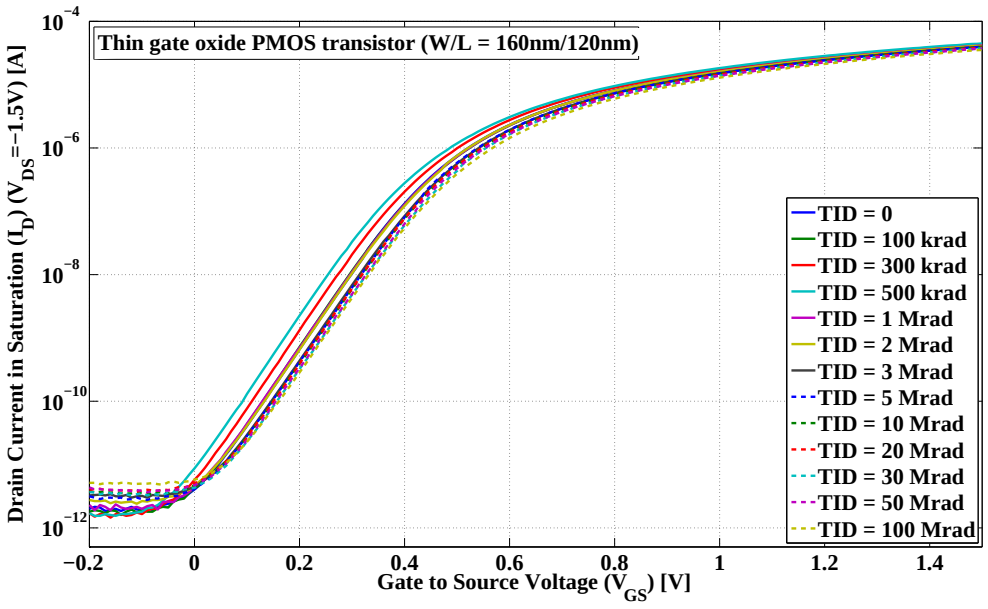

Figure 2.10: Evolution of the transfer characteristic with the TID for a minimum size ($W = 0.16\,\mu m$, $L = 0.12\,\mu m$), thin gate oxide, *p*-channel transistor manufactured in 130 nm technology node.

Results shown in Fig. 2.11 and Fig. 2.12 are presented in order to compare the radiation tolerance of the thin and thick gate oxide transistors manufactured in the same technology. The transfer characteristics have been measured for the minimum size ($W = 0.36\,\mu m$, $L = 0.24\,\mu m$) *n*- and *p*-channel transistors biased to operate in saturation. The increase of the leakage current in the thick gate oxide NMOS transistors is large, over four orders of magnitude. Due to the decrease of the carrier mobility, the degradation of the subthreshold slope and the gain is significant. The radiation induced increase of the leakage current in the thick oxide PFET is also visible but much smaller, only one order of magnitude at maximum doses.

2.5.2 Threshold voltage shift

The radiation induced threshold voltage shift is expected to occur in all measured transistors, regardless of their type. The threshold voltage shift (ΔV_{th}) is calculated as the difference between the value of the voltage extracted from the characteristic after irradiation up to a certain dose, $V_{th(TID)}$, and its pre-irradiation value, $V_{th(prerad)}$. Some of the collected results are presented in Figs. 2.13, 2.14, 2.15 and 2.16.

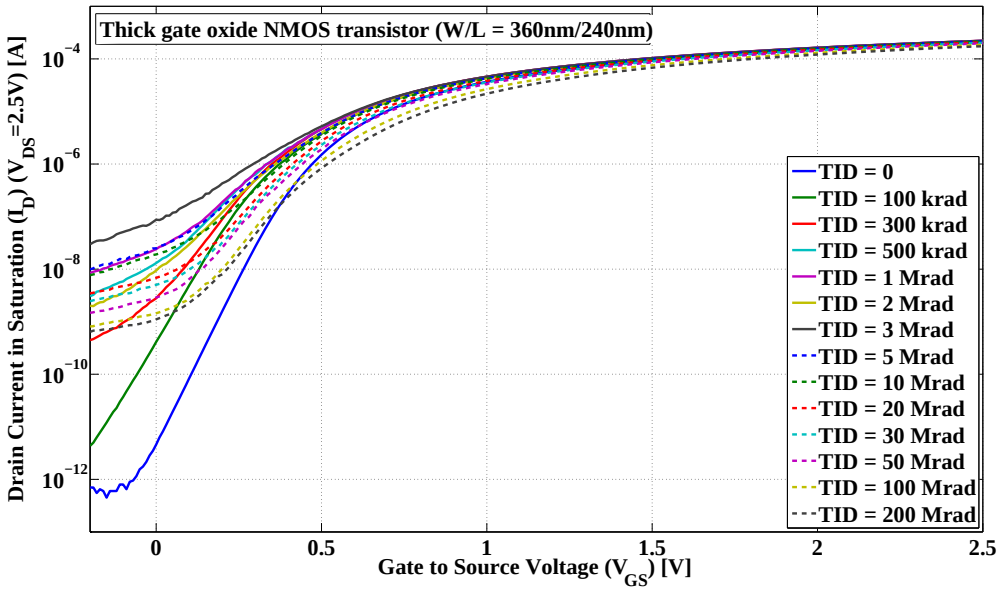

Figure 2.11: Evolution of the transfer characteristic with the TID for a minimum size ($W = 0.36\,\mu m$, $L = 0.24\,\mu m$), thick gate oxide, *n*-channel transistor manufactured in 130 nm technology node.

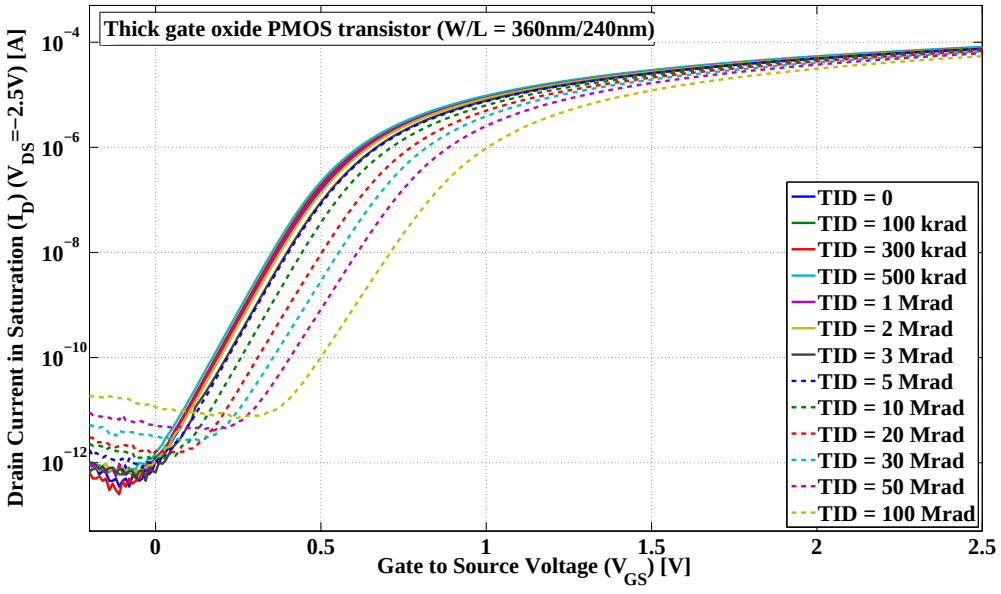

Figure 2.12: Evolution of the transfer characteristic with the TID for a minimum size ($W = 0.36\,\mu m$, $L = 0.24\,\mu m$), thick gate oxide, *p*-channel transistor manufactured in 130 nm technology node.

Among the thin oxide *n*-channel transistors (Fig. 2.13) the biggest change of the threshold voltage is observed for short channel devices. The magnitude of the effect decreases together with the transistor width, for instance: $\Delta V_{th} \approx -80\,\mathrm{mV}$ for $W = 0.16\,\mu\mathrm{m}$, $\Delta V_{th} \approx -42\,\mathrm{mV}$ for $W = 0.64\,\mu\mathrm{m}$ and $\Delta V_{th} \approx -20\,\mathrm{mV}$ for $W = 2.0\,\mu\mathrm{m}$. It is also worth noting that this effect is almost negligible for longer transistors ($L = 1\,\mu\mathrm{m}$ or higher), around $-8\,\mathrm{mV}$ for NFET with $W/L = 10\,\mu\mathrm{m}/1\,\mu\mathrm{m}$. No notable change in the value of V_{th} of the ELT is observed.

The thick oxide transistors are expected to be more sensitive to the TID effects causing the V_{th} shift, than the transistors with the thin gate oxide. These expectations are confirmed by the results presented in Fig. 2.14. In case of thick gate oxide devices a significant drop of the threshold voltage occurs immediately after the start of irradiation. For the minimum size NFET the threshold voltage shift exceeds 200 mV. In the transistors with high W/L ratios and transistors with long channels the effect becomes less significant. Above the TID of around $3-5\,\mathrm{Mrad}$ the threshold voltage shift decreases again due to the expected rebound effect. The value of ΔV_{th} measured at 200 Mrad is usually between $50-100\,\mathrm{mV}$.

The results obtained from the irradiation test of the thin oxide *p*-channel transistors are shown in Fig. 2.15. One should note that for relatively small doses, the threshold voltage becomes more positive (its absolute value decreases) resulting in an unexpected rebound in the V_{th} characteristic. For a minimum size MOS transistor the threshold voltage can shift even by 40 mV. Smaller rebounds are also observed for other tested short channel transistors, but the effect becomes less significant together with the increase of the transistor width. After exceeding the dose of around 1 Mrad the absolute value of the threshold voltage increases, resulting in the shift between 6 mV and 40 mV at TID of 100 Mrad.

Figure 2.16 presents the results collected from the measurement of the thick oxide PMOS transistors. All short channel devices suffer from a very high threshold voltage shift (between 330 mV and 370 mV measured at 100 Mrad). The shift observed in long channels (1 μm and above) is $100\,\mathrm{mV}-150\,\mathrm{mV}$ lower.

2.5.3 Leakage current

The leakage current is considered to be a very serious issue especially in NMOS transistors fabricated in a *p*-type silicon wafer, but according to the results collected from the TID3, leakage current can also occur in thick gate oxide PMOS transistors.

Figures 2.17, 2.18 and 2.19 present the measured evolution of the leakage current with the TID in thin and thick gate oxide *n*-channel transistors, and thick gate oxide *p*-channel transistors, respectively.

Figure 2.17 shows the evolution of the leakage current in the thin gate oxide NFETs. One can immediately notice that the pre-irradiation value of the leakage current in all the narrow transistors is low, in the range of few hundreds of pA. In the case of longer transistors ($L = 1\,\mu$m and $L = 10\,\mu$m) the pre-irradiation value is one order of magnitude higher. The rapid increase of the leakage current occurs already above the TID of 100 krad with the maximum at around 30 Mrad – 50 Mrad. Typically, the increase is in the range of one order of magnitude for short channel transistors and of factor 2.5 – 3 for transistors with a long channel. The leakage current in ELT is constant despite the TID.

As expected, the increase of the leakage current is much higher in the case of the thick gate oxide NFETs (Fig. 2.18). Although, the initial, pre-irradiation values are low, below 10 pA for all the measured devices, the overall change can reach 3 – 4 orders of magnitude for short channel transistors. The thick gate oxide transistors with long channels are less sensitive to the TID effects and this results in the leakage current increase only by two orders of magnitude. No change in the value of the leakage current is observed in case of the thick gate oxide ELT.

The initial value of the leakage current for small transistors is on the level of single pA and few tens of pA for longer transistors 2.19. The thick gate oxide PMOS transistors behave normally (no change in the leakage current) up to around 1 Mrad. Above this value a monotonic increase of the leakage current is observed. The change is however very small, in the range of one order of magnitude. The post-irradiation value of the leakage current is still below 1 nA.

2.5.4 On-current

The on-current (I_{on}), or equivalently the on-resistance (R_{on}), of a transistor can significantly change with the TID. The on-resistance is a MOSFET parameter which is mainly responsible for power losses in the switches commonly used in DC-DC converters. The decrease of the on-current means the increase of on-resistance and hence increase of power losses. This issue will be discussed in detail in the next chapter. A percentage change of the on-current is defined in the following way:

$$\frac{\Delta I_{on}}{I_{on(prerad)}} = \frac{I_{on(TID)} - I_{on(prerad)}}{I_{on(prerad)}} \cdot 100\,\%, \tag{2.13}$$

where $I_{on(TID)}$ is the value of the on-current measured for a given transistor and for a given dose, while $I_{on(prerad)}$ is its pre-irradiation value ($I_{on(TID)}$ for TID $= 0$).

Figure 2.20 presents how the on-current evolves with the TID in tested thin gate oxide *n*-channel transistors. The on-current depends on the value of V_{th}, thus according to Fig. 2.13, short channel transistors are going to be affected more strongly than long transistors. This is fully confirmed by the obtained test results. For the minimum size NFET, the value of $\Delta I_{on}/I_{on(prerad)}$ exceeds 10 % for a dose of 5 Mrad. For high doses, I_{on} starts decreasing. This occurs due to charge trapped in the Si/SiO_2 interface, which affects the V_{th} of the NFETs.

The effect of on-current change is clearly visible in the thick gate oxide *n*-channel transistors (Fig. 2.21), obviously due to a higher threshold voltage change. A small increase of I_{on} is observed for small doses, while for high doses the on-current starts to drop quite rapidly. Depending on the transistor size, the percentage change measured at the dose of 200 Mrad is between 12 % and 18 %, with respect to the pre-irradiation value of the on-current.

The evolution of the on-current in irradiated thin gate oxide *p*-channel transistors is shown in Fig. 2.22. As expected, the minimum size transistor used for the test tends to be the most sensitive device among all of them. The value of $\Delta I_{on}/I_{on(prerad)}$ in this case can vary between around $+7$ % and -16 %. In short channel devices, after an initial drop, the absolute value of the on-current above the TID of 1 Mrad starts decreasing in all transistors. Wider transistors and transistors with the long channels are less sensitive.

A strong effect is observed in thick gate oxide PFETs (Fig. 2.23). In general, as expected the short channel transistors are affected the most with the percentage change reaching -30 %. The transistors with long channels are less sensitive, however the measured $\Delta I_{on}/I_{on(prerad)}$ is still big (around -20 %). A small rebound around 500 krad is related to the rebound observed in ΔV_{th} characteristic shown in Fig. 2.16.

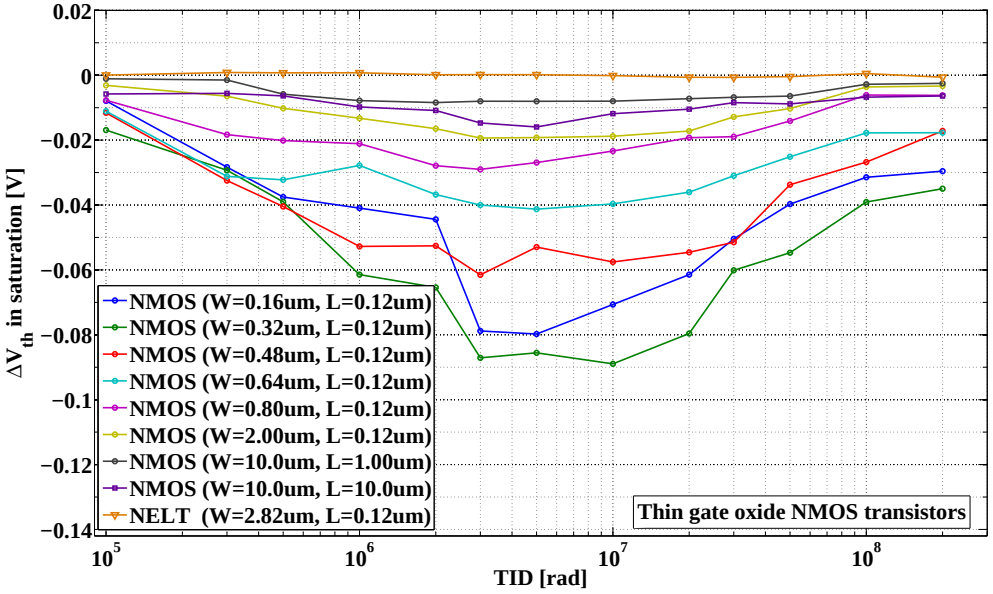

Figure 2.13: Evolution of the threshold voltage shift (ΔV_{th}) with the TID for thin gate oxide, *n*-channel transistors manufactured in 130 nm technology node.

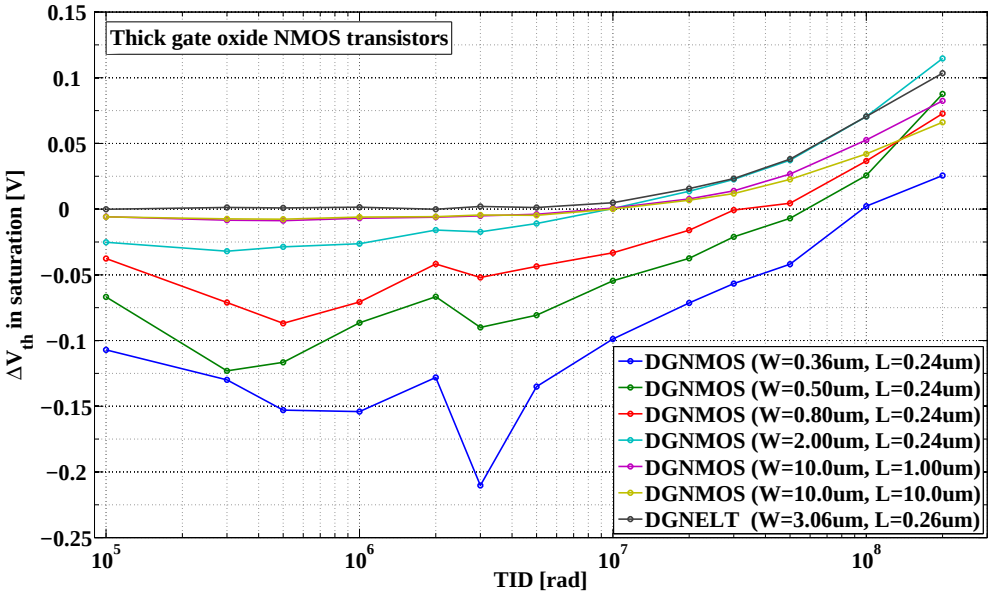

Figure 2.14: Evolution of the threshold voltage shift (ΔV_{th}) with the TID for thick gate oxide, *n*-channel transistors manufactured in 130 nm technology node.

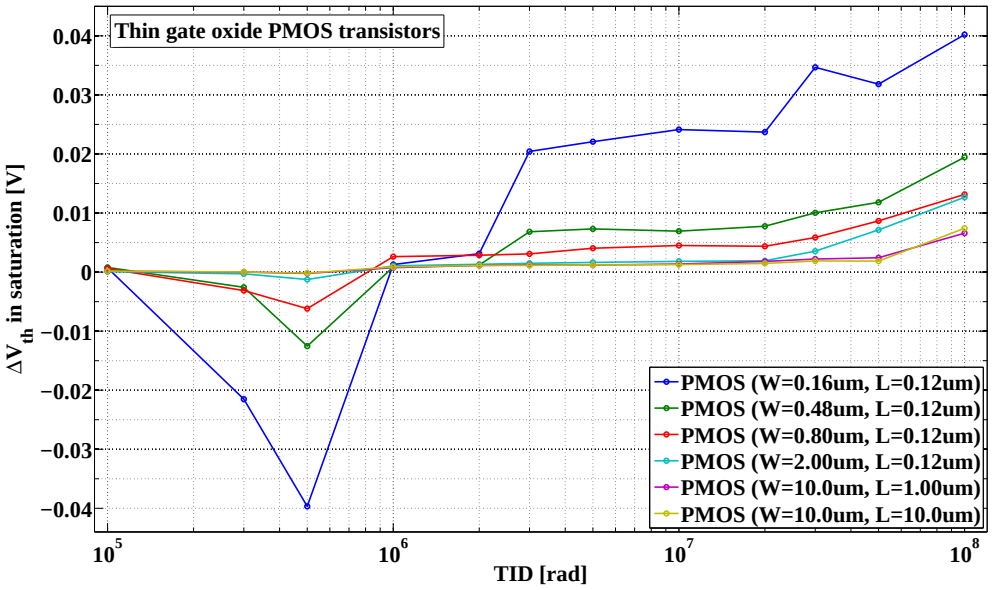

Figure 2.15: Evolution of the threshold voltage shift (ΔV_{th}) with the TID for thin gate oxide, *p*-channel transistors manufactured in 130 nm technology node.

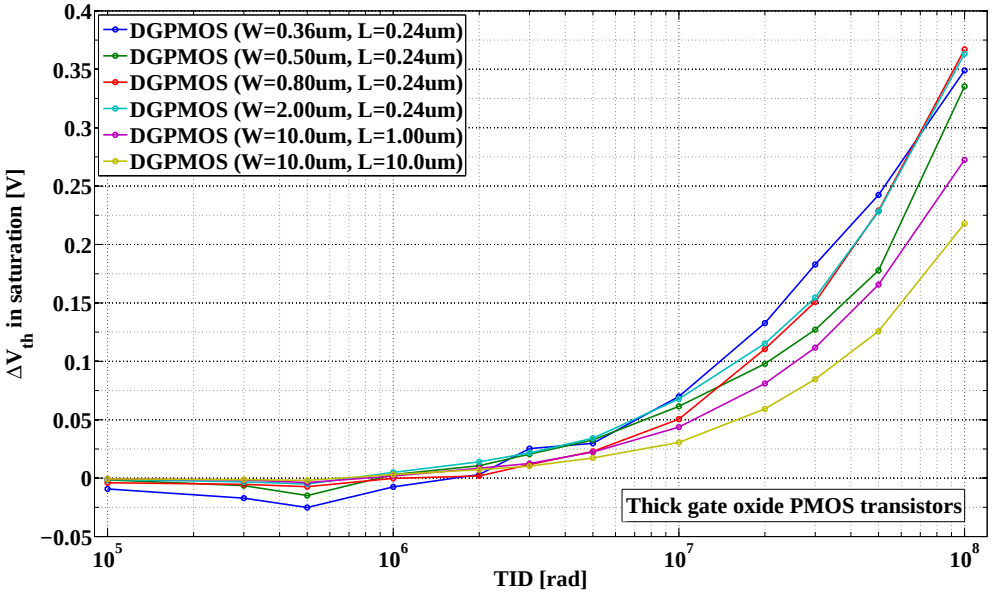

Figure 2.16: Evolution of the threshold voltage shift (ΔV_{th}) with the TID for thick gate oxide, *p*-channel transistors manufactured in 130 nm technology node.

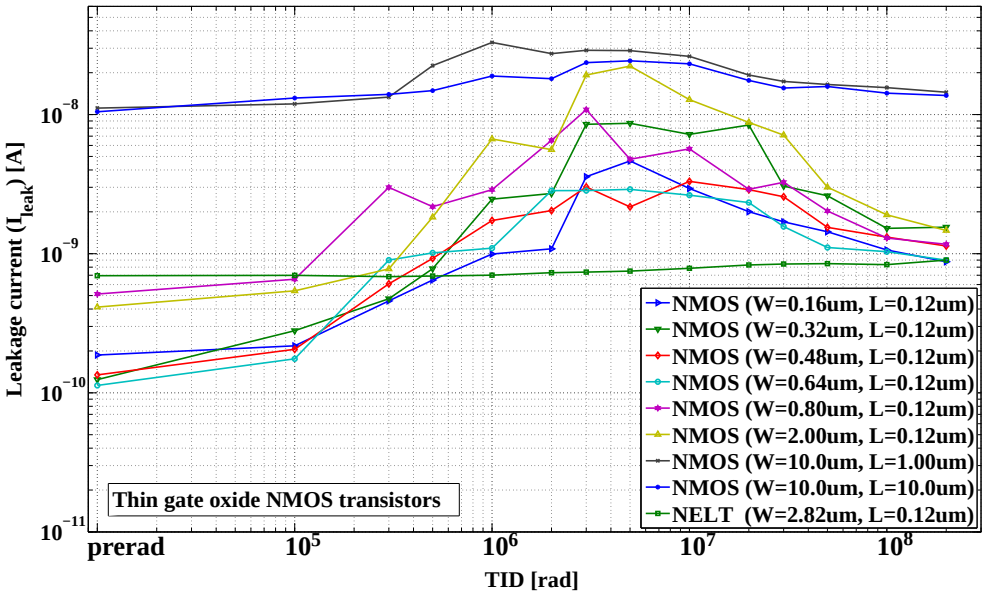

Figure 2.17: Evolution of the leakage current (I_{leak}) with the TID for thin gate oxide, *n*-channel transistors manufactured in 130 nm technology node.

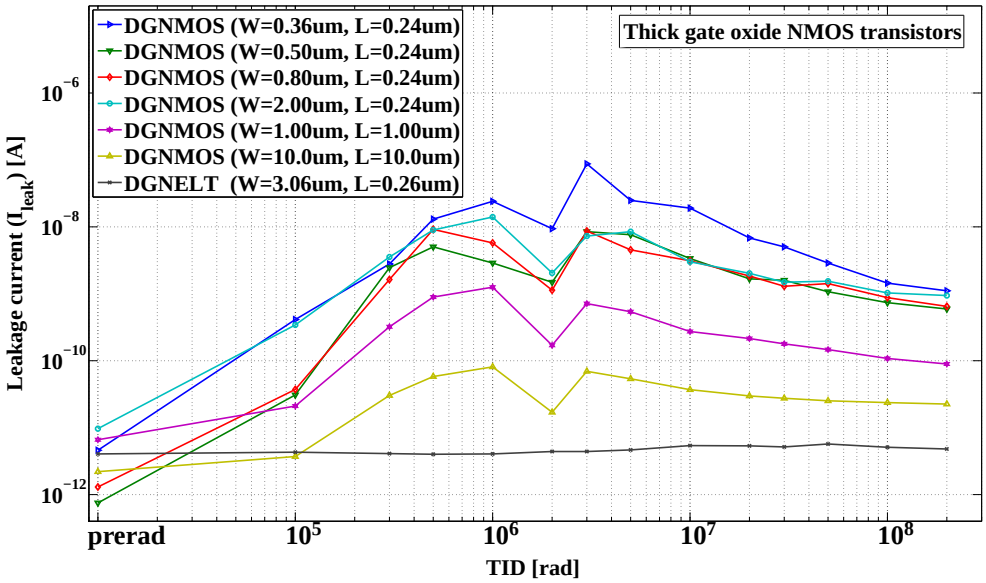

Figure 2.18: Evolution of the leakage current (I_{leak}) with the TID for thick gate oxide, *n*-channel transistors manufactured in 130 nm technology node.

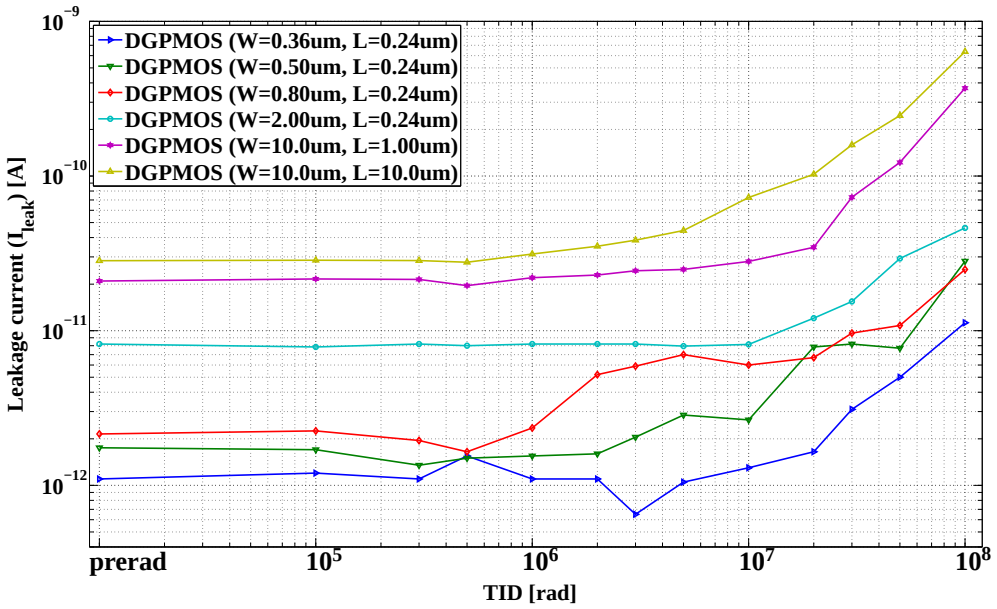

Figure 2.19: Evolution of the leakage current (I_{leak}) with the TID for thick gate oxide, *p*-channel transistors manufactured in 130 nm technology node.

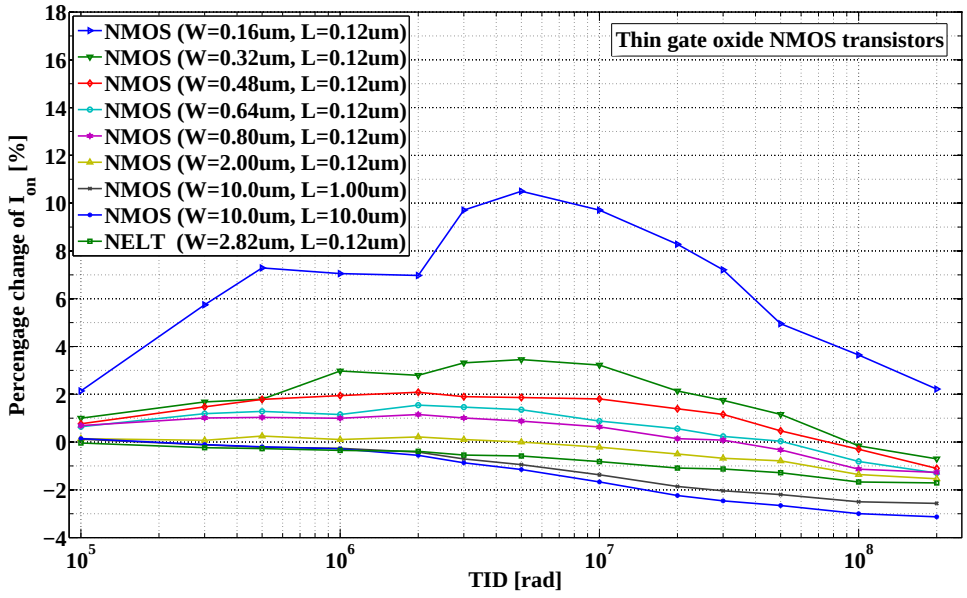

Figure 2.20: Percentage change of the on-current (I_{on}) with respect to its pre-irradiation value as a function of the TID for thin gate oxide, *n*-channel transistors manufactured in 130 nm technology node.

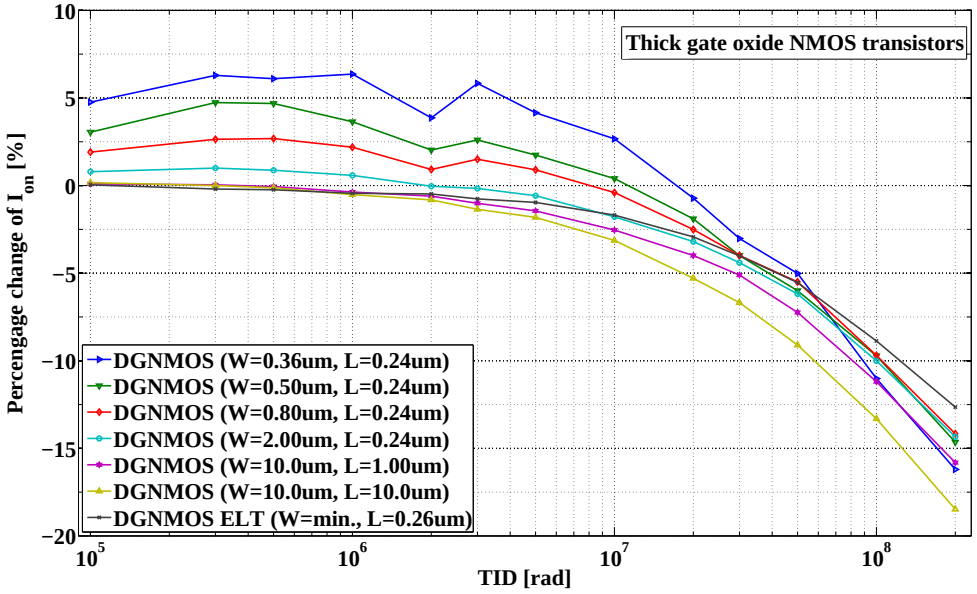

Figure 2.21: Percentage change of the on-current (I_{on}) with respect to its pre-irradiation value as a function of the TID for thick gate oxide, *n*-channel transistors manufactured in 130 nm technology node.

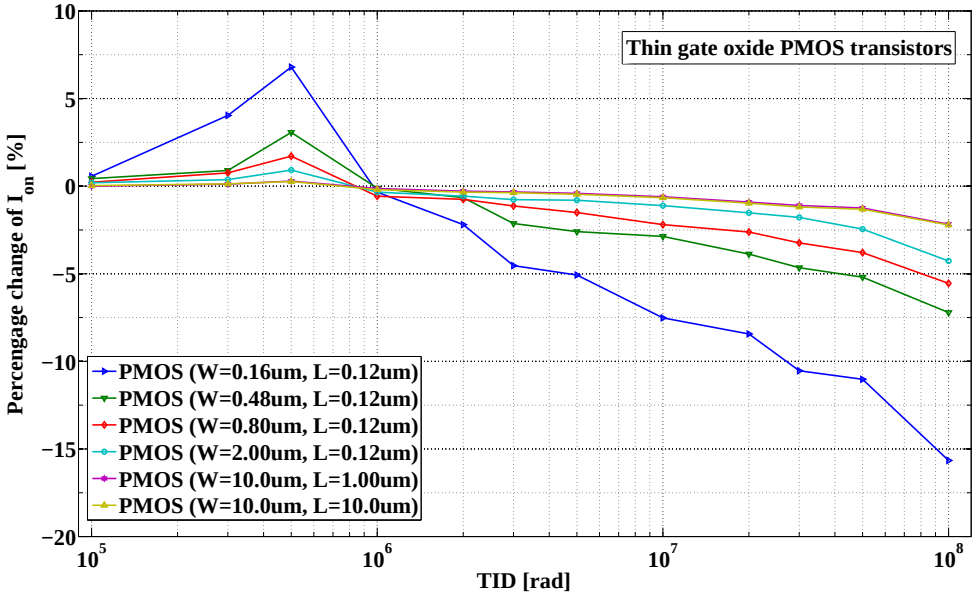

Figure 2.22: Percentage change of the on-current (I_{on}) with respect to its pre-irradiation value as a function of the TID for thin gate oxide, *p*-channel transistors manufactured in 130 nm technology node.

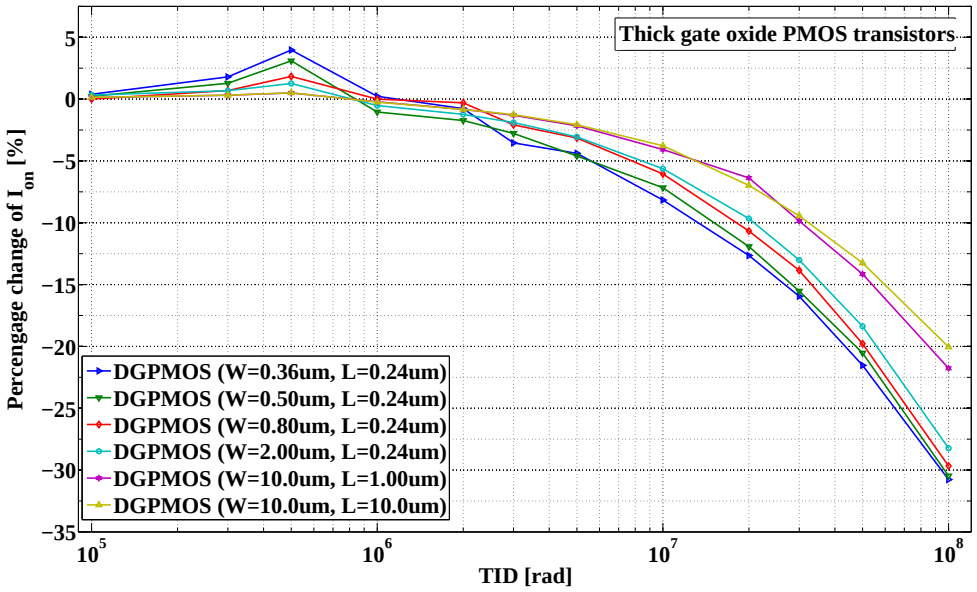

Figure 2.23: Percentage change of the on-current (I_{on}) with respect to its pre-irradiation value as a function of the TID for thick gate oxide, *p*-channel transistors manufactured in 130 nm technology node.

2.6 Radiation tolerance of 90 nm CMOS9FLP/RF technology

Although the IBM 90 nm CMOS process is not currently considered as an option for the electronics upgrade in the future ID, performing the irradiation tests helps to understand the evolution of the intrinsic radiation tolerance with the technology scaling. The chip used in the test has already been presented in Section 2.3.1. The block A of the TID90 containing PMOS transistors was irradiated up to a TID of 200 Mrad, while the NMOS transistors up to TID of 50 Mrad.

2.6.1 Transfer characteristics

Figures 2.24, 2.25, 2.26 and 2.27 show the transfer characteristics measured for the minimum size thin and thick gate oxide *n*- and *p*-channel transistors.

The I_D-V_{GS} curves presented in Fig. 2.24 were measured for the thin gate oxide *n*-channel transistor with W/L ratio of ($W = 0.12\,\mu$m, $L = 0.10\,\mu$m). The leakage current measured at $V_{GS} = 0$ increases by five orders of magnitude during irradiation, from around

0.4 pA up to around 120 nA. However, it is worth noting that the value of the leakage current is lower (by three orders of magnitude) than in the case of minimum size NFETs fabricated in the 130 nm process.

The minimum size thin gate oxide *p*-channel transistor (Fig. 2.25) is almost completely insensitive to the radiation effects causing the variation of the leakage current. Only a two-fold increase of the leakage current is observed and the post-irradiation value (at 200 Mrad) still remains in the range of few pA.

Figure 2.26 shows the evolution of the transfer characteristic of the minimum size, thick gate oxide NFET. A measured increase in the leakage current is very high, around six orders of magnitude, with a maximum around the TID of 2 Mrad. From the presented plot a degradation of the subthreshold slope factor is also clearly visible.

The family of I_D-V_{GS} curves measured for a thick gate oxide *p*-channel transistor is shown in Fig. 2.27. The measured leakage current increases by two orders of magnitude, ten times more than in the case of the minimum size transistor manufactured in 130 nm technology. The shift of the characteristics due to the threshold voltage shift is also clearly visible.

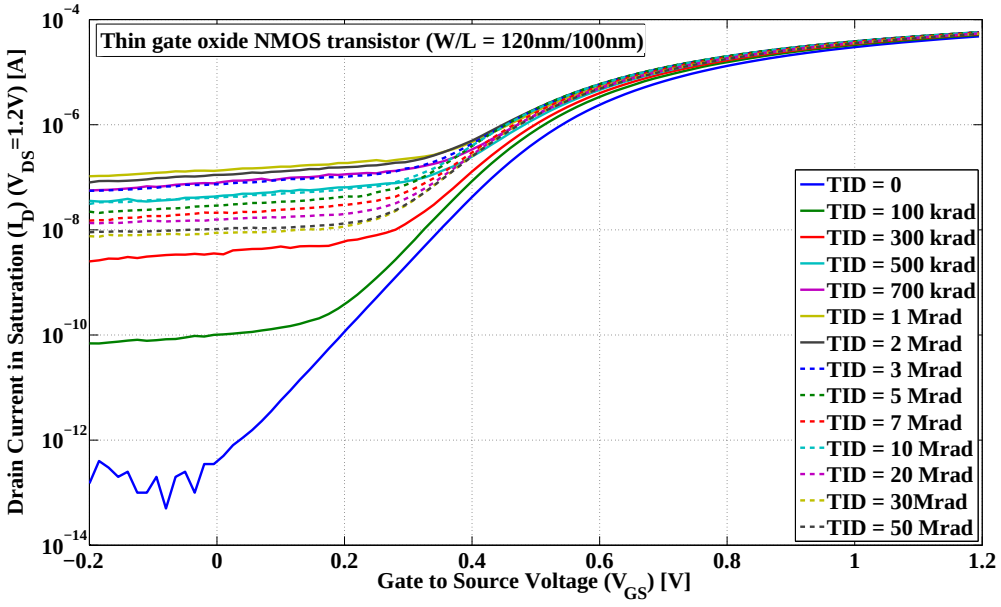

Figure 2.24: Evolution of the transfer characteristic with the TID for a minimum size ($W = 0.12\,\mu$m, $L = 0.10\,\mu$m), thin gate oxide, *n*-channel transistor (90 nm technology node).

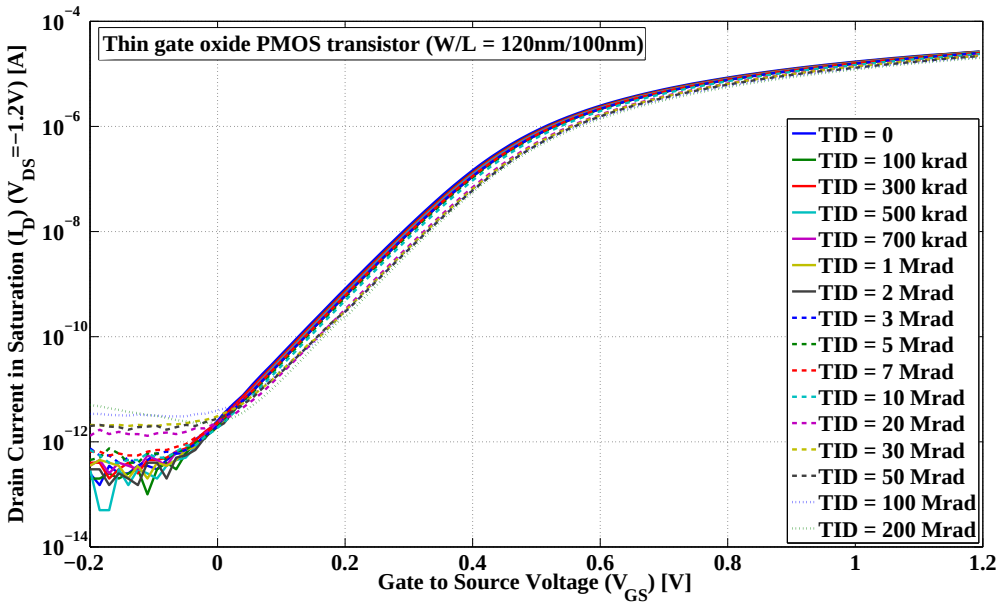

Figure 2.25: Evolution of the transfer characteristic with the TID for a minimum size ($W = 0.12\,\mu m$, $L = 0.10\,\mu m$), thin gate oxide, *p*-channel transistor (90 nm technology node).

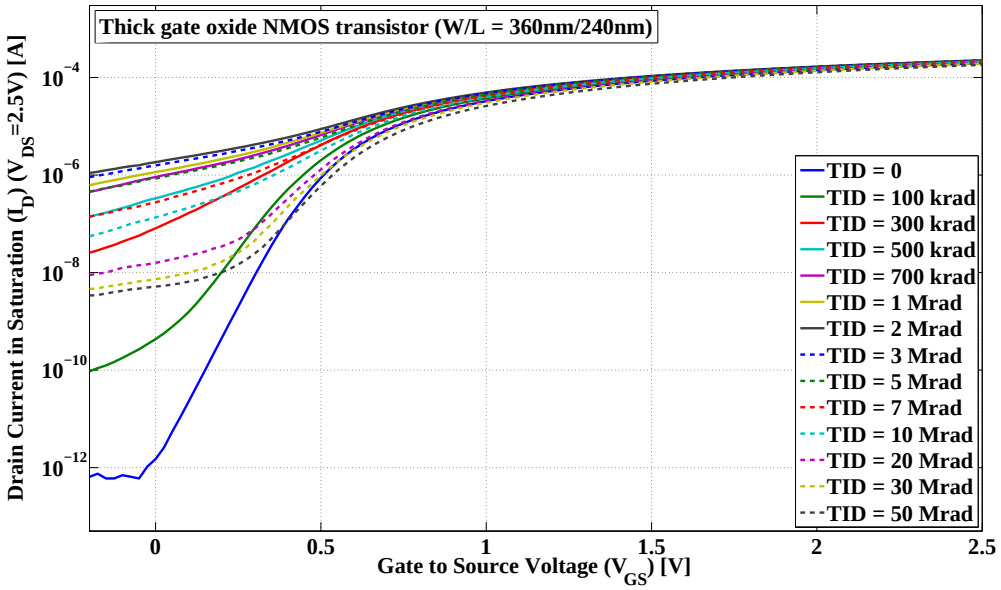

Figure 2.26: Evolution of the transfer characteristic with the TID for a minimum size ($W = 0.36\,\mu m$, $L = 0.24\,\mu m$), thick gate oxide, *n*-channel transistor (90 nm technology node).

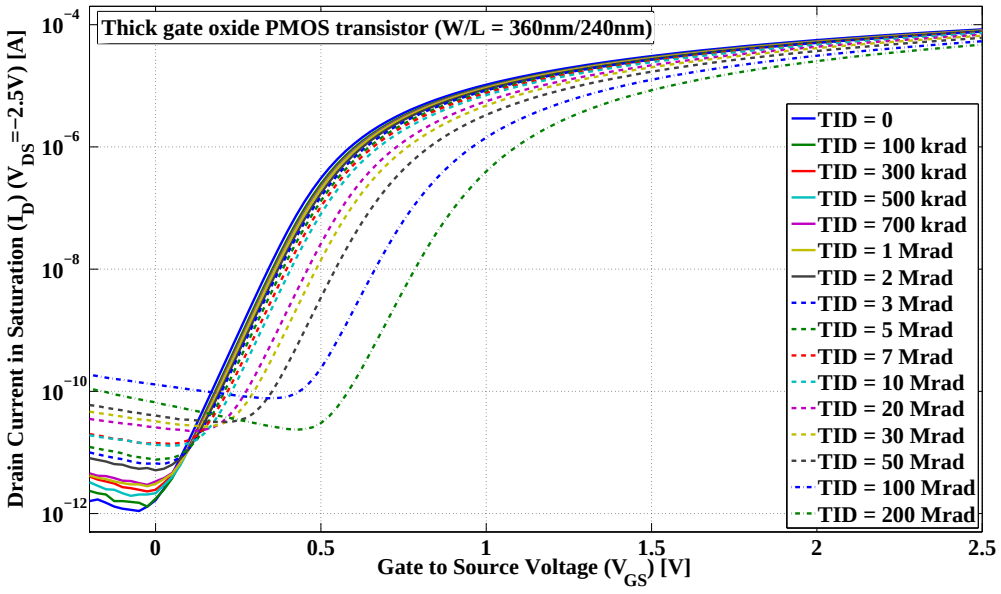

Figure 2.27: Evolution of the transfer characteristic with the TID for a minimum size ($W = 0.36\,\mu$m, $L = 0.24\,\mu$m), thick gate oxide, *p*-channel transistor (90 nm technology node).

2.6.2 Threshold voltage shift

The transistors manufactured in the 90 nm process are highly susceptible to the TID effects. The evolution of the radiation induced V_{th} shift measured for the transistors laid out on the TID90 test chip is presented in Figs. 2.28, 2.29, 2.30 and 2.31.

Figure 2.28 shows the evolution of the threshold voltage shift in the thin gate oxide *n*-channel transistors. The V_{th} shift observed for a minimum size transistor exceeds 100 mV and it is 10 mV higher than the shift measured for the minimum size transistor fabricated in 130 nm technology. The measurement confirms again that the minimum size transistors are the most sensitive to the radiation induced threshold voltage shift. The shift observed in long transistors ($L = 1\,\mu$m and higher) is in order of a few mV, so almost negligible.

The results collected from the measurements of the thick gate oxide NMOS transistors are shown in Fig. 2.29. One can immediately note the shift caused by the ionising radiation for this technology is larger than for the previously discussed process. The threshold voltage measured for the minimum size NMOS transistor is 640 mV, which is more than a half of the nominal supply voltage foreseen for this technology. As expected, the V_{th} shift decreases with the increase of the width of the transistors ($\Delta V_{th} \approx 590$ mV for $W = 0.72\,\mu$m and $\Delta V_{th} \approx 50$ mV for $W = 10\,\mu$m). NMOS transistors with longer channels are affected to a lesser degree. In this case the measured threshold voltage shift is only

around $20-40$ mV.

The V_{th} characteristics of the thin oxide *p*-channel transistors are shown in Fig. 2.30. The minimum size transistor suffers from the highest shift of 73 mV. In longer transistors (L=1 μm and L=10 μm) the measured shift is around 25 mV. For PFETs with constant width ($W = 10$ μm) the effect scales down insignificantly with the increase of the channel length.

The threshold voltage shift measured for the thick gate oxide *p*-channel transistors is presented in Fig. 2.31. The absolute value of V_{th} starts to increase rapidly above the TID of 1 Mrad. The shift of the threshold voltage measured for the minimum length transistors at TID of 200 Mrad is between 450 mV and 500 mV. Transistors with longer channels behave slightly better, but the measured shift is still very high, around 400 mV.

2.6.3 Leakage current

The leakage current evolution with the TID measured for the thin and thick gate oxide transistors laid out on the TID90 chip is shown in Figs. 2.32, 2.33, 2.34. Due to the fact, that no significant effect on the leakage in thin gate oxide *p*-channel transistors has been observed, they have been omitted in this section.

Figure 2.32 shows the leakage current characteristics of the irradiated thin gate oxide *n*-channel transistors. One can note a very low pre-irradiation leakage current in short transistors which is below 1 pA. These values are roughly two orders of magnitude lower comparing to the results from the 130 nm process. The leakage current measured in long FETs ($L = 1$ μm and $L = 10$ μm) before irradiation is 6 nA and 4 nA, respectively. This is half of the 10 nA measured for the identical transistors in the previously discussed technology. The leakage current in thin gate oxide NFETs increases rapidly after the start of irradiation and reaches its maximum value at the TID of around $1-2$ Mrad. The biggest increase was measured for the minimum size device, six orders of magnitude, and for the transistor with $W/L = 0.24\,\mu\text{m}/0.10\,\mu\text{m}$, four orders of magnitude was measured. The measurement of the ELT leakage current shows that it does not change with the dose.

Results collected from the measurements of the thick gate oxide *n*-channel transistors are shown in Fig. 2.33. As expected, also in this case the increase of the leakage current is significant, with a maximum around the TID of $1-2$ Mrad. The radiation induced increase of the leakage current is between five and six orders of magnitude in almost all tested transistors, and reaches 1 μA. Only in the case of the device with the long channel ($L = 10$ μm) was the difference between the pre-irradiation and the maximum value limited to four orders of magnitude. Similarly to the thin gate oxide transistors, also

in case of thick gate oxide ELT, no change in the leakage was observed.

A small increase of the leakage current at high doses has also been observed in thick gate oxide PMOS transistors. The results are presented in Fig. 2.34. The initial (pre-irradiation) value of the leakage current is very small (of the order of a few or a few tens of pA). Due to radiation this value can increase by 1–2 orders of magnitude, depending on the transistor dimensions.

2.6.4 On-current

The on-current is the last transistor parameter for which the evolution with the TID is presented in this chapter. The results collected from the measurements of the regular-V_{th} thin and thick gate oxide NFETs and PFETs are presented in Figs. 2.35, 2.36, 2.37 and 2.38.

The results shown in Fig. 2.35 prove that the radiation induced variation of the on-current in the NMOS devices is a very serious issue. The observed change in the case of the minimum size transistor reaches up to 20 % at the TID of $2-5$ Mrad. The long transistors and the ELT are not susceptible to the TID, however a small drop of 2 % is observed for very high doses (50 Mrad).

The on-current depends on the threshold voltage, hence the effect of radiation induced variation of on-current is expected to be much larger in the thick gate oxide NFETs (Fig. 2.36). Due to the decrease of V_{th} at lower doses, the on-current increases and reaches maximum around TID of 2 Mrad. For doses higher than few Mrad the on-current starts to decrease. The highest variation is observed in the minimum size transistor (between $+14$ % and -8 %). The I_{on} characteristics measured for long channel transistors are flat but above 10 Mrad a rapid drop has been observed.

Figure 2.37 shows the evolution of the on-current in the thin gate oxide *p*-channel transistors. In all measured devices the on-current tends to monotonically decrease with the TID. Typically, the smallest device is the most susceptible to the ionisation effects, thus percentage change of I_{on} reaches -25 %. The effect is reduced with the increase of the channel length. The measured $\Delta I_{on}/I_{on}$ for transistors with $L \geq 1\,\mu$m is only about -5 %.

A large monotonic drop of the on-current has been observed for thick gate oxide PMOS transistors (Fig. 2.38). The measured variation of on-current at 200 Mrad, in comparison with the pre-irradiation value is as high as -44 % for the minimum size device and -37 % for the long transistor.

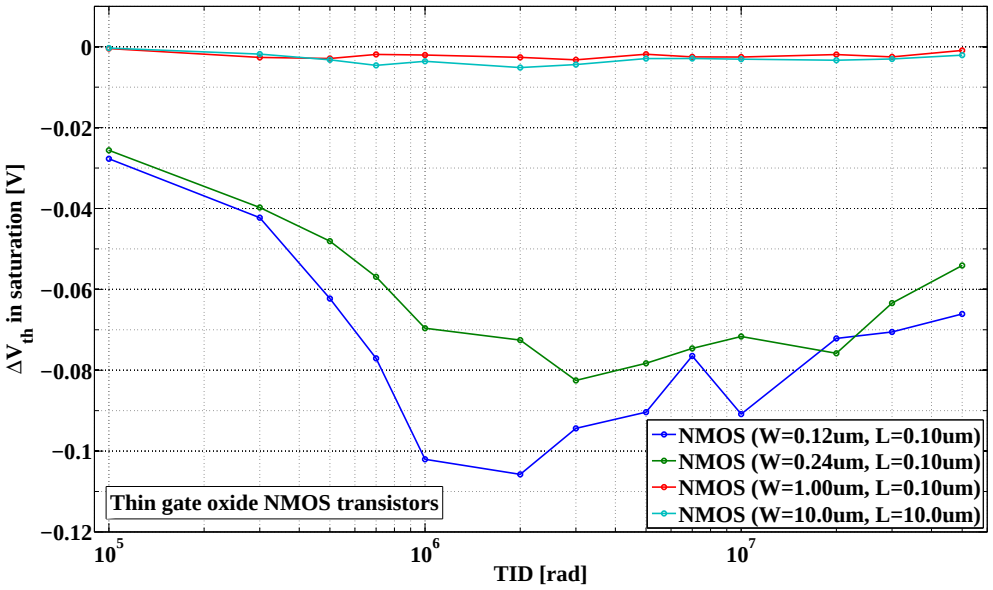

Figure 2.28: Evolution of the threshold voltage shift (ΔV_{th}) with the TID for thin gate oxide, *n*-channel transistors manufactured in 90 nm technology node.

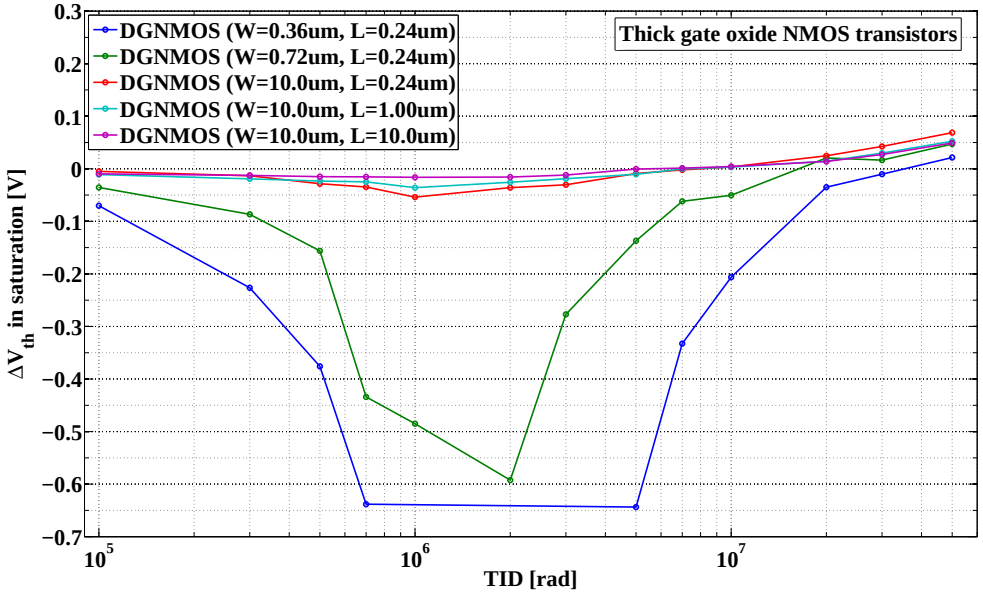

Figure 2.29: Evolution of the threshold voltage shift (ΔV_{th}) with the TID for thick gate oxide, *n*-channel transistors manufactured in 90 nm technology node.

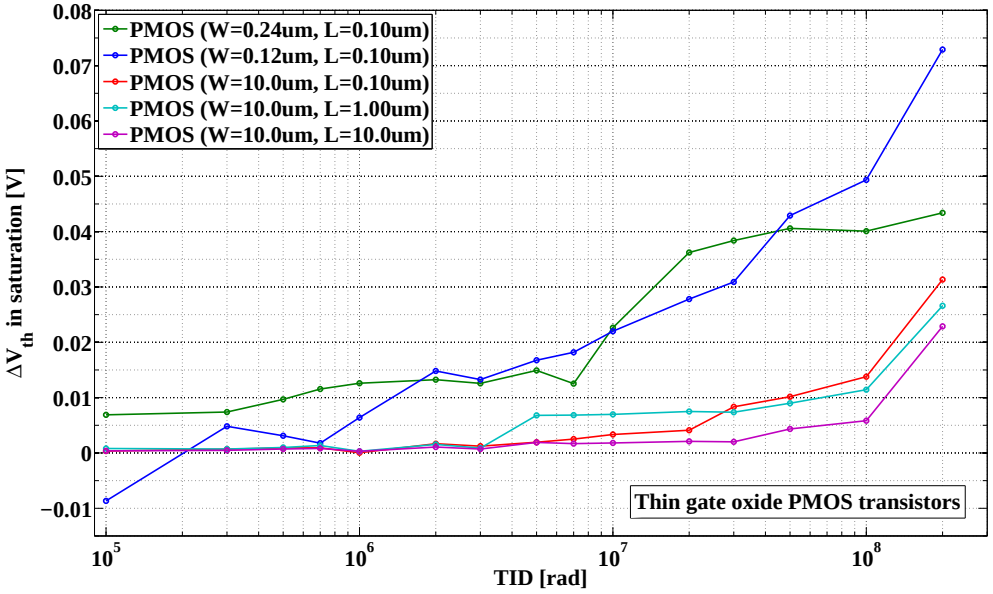

Figure 2.30: Evolution of the threshold voltage shift (ΔV_{th}) with the TID for thin gate oxide, *p*-channel transistors manufactured in 90 nm technology node.

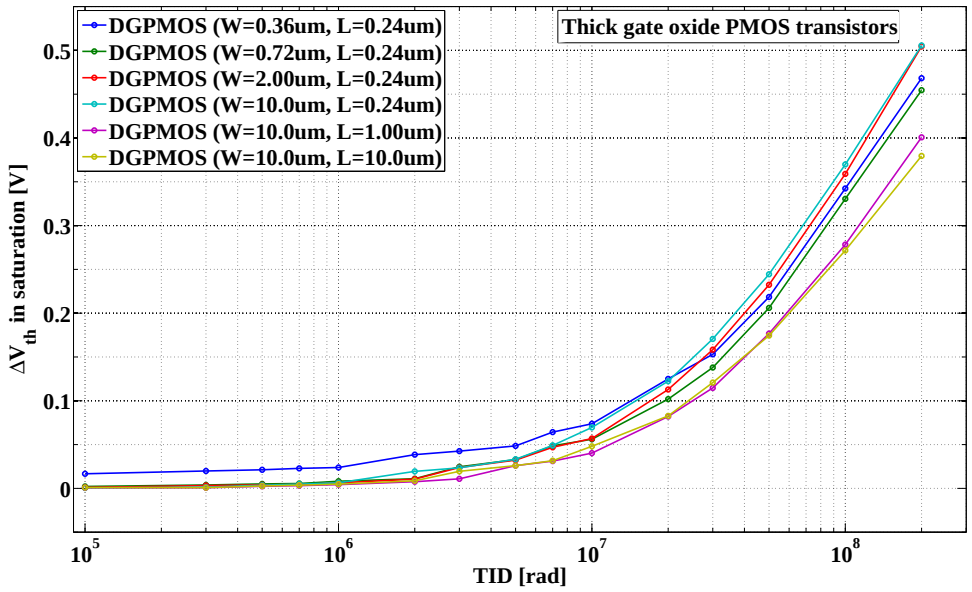

Figure 2.31: Evolution of the threshold voltage shift (ΔV_{th}) with the TID for thick gate oxide, *p*-channel transistors manufactured in 90 nm technology node.

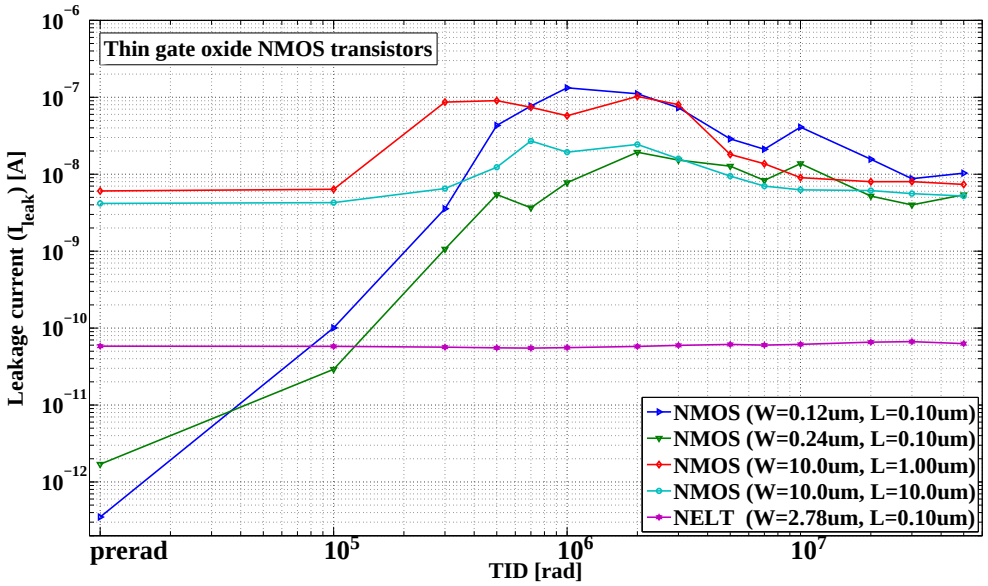

Figure 2.32: Evolution of the leakage current (I_{leak}) with the TID for thin gate oxide, *n*-channel transistors manufactured in 90 nm technology node.

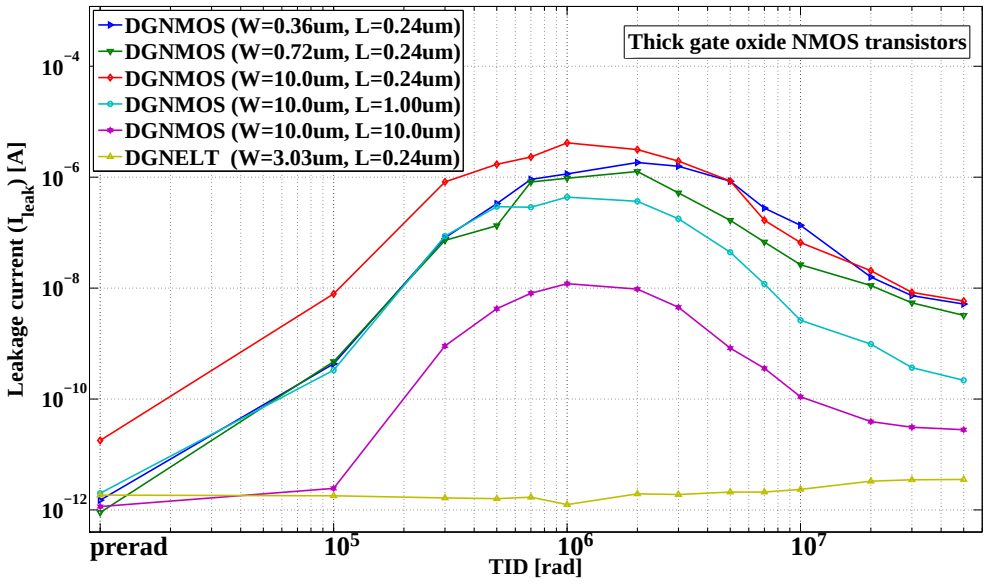

Figure 2.33: Evolution of the leakage current (I_{leak}) with the TID for thick gate oxide, *n*-channel transistors manufactured in 90 nm technology node.

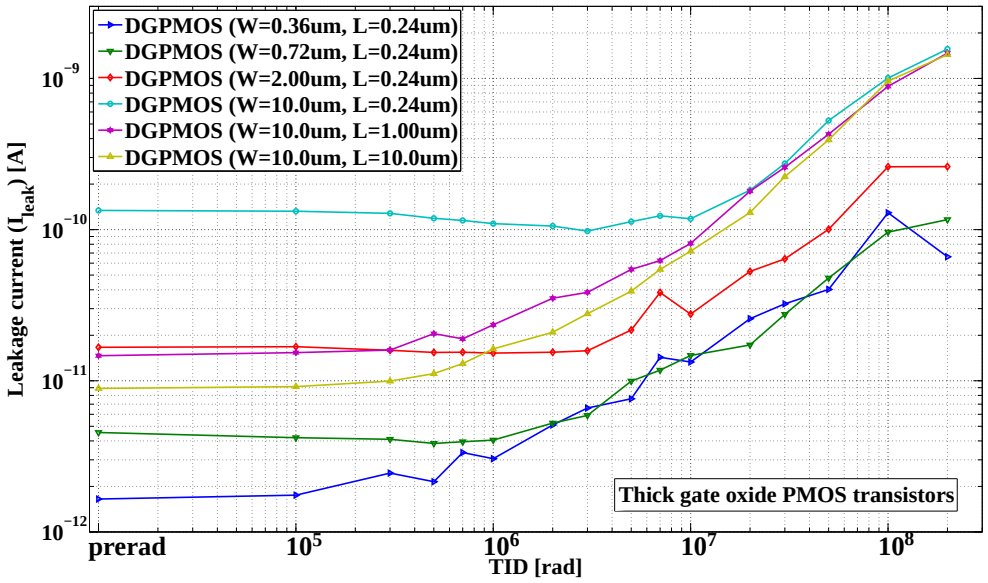

Figure 2.34: Evolution of the leakage current (I_{leak}) with the TID for thick gate oxide, *p*-channel transistors manufactured in 90 nm technology node.

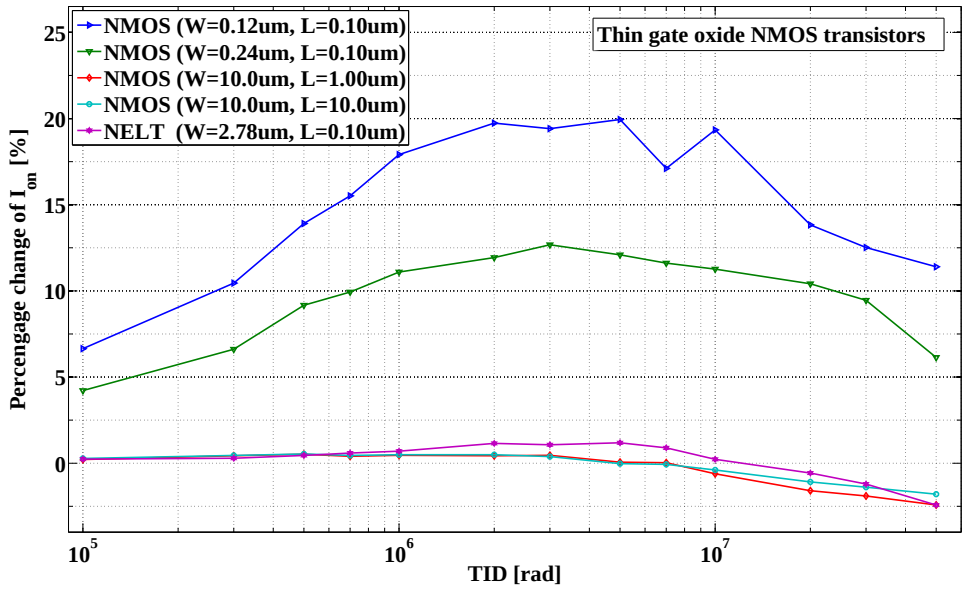

Figure 2.35: Percentage change of the on-current (I_{on}) with respect to its pre-irradiation value as a function of the TID for thin gate oxide *n*-channel transistors manufactured in 90 nm technology node.

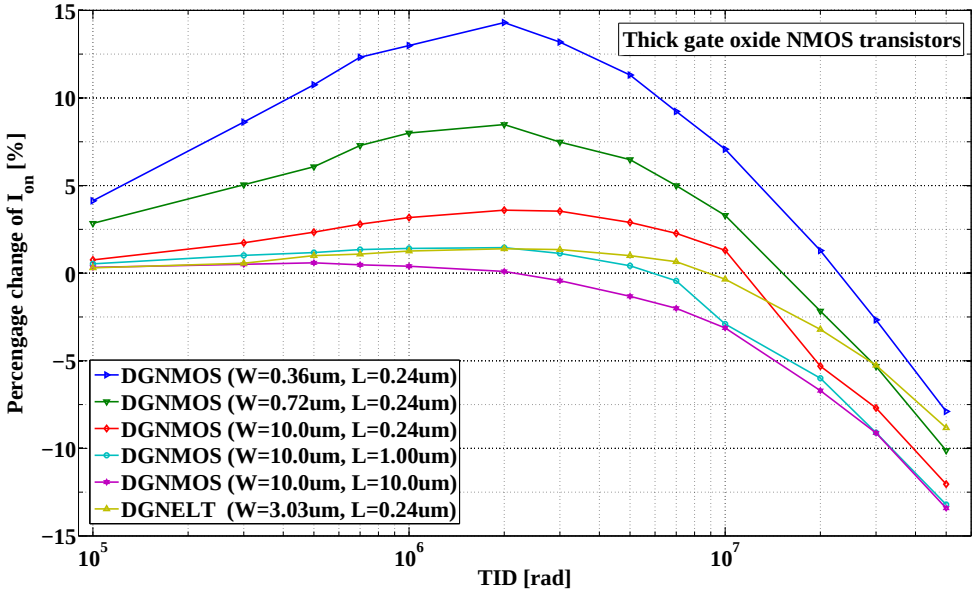

Figure 2.36: Percentage change of the on-current (I_{on}) with respect to its pre-irradiation value as a function of the TID for thick gate oxide, *n*-channel transistors manufactured in 90 nm technology node.

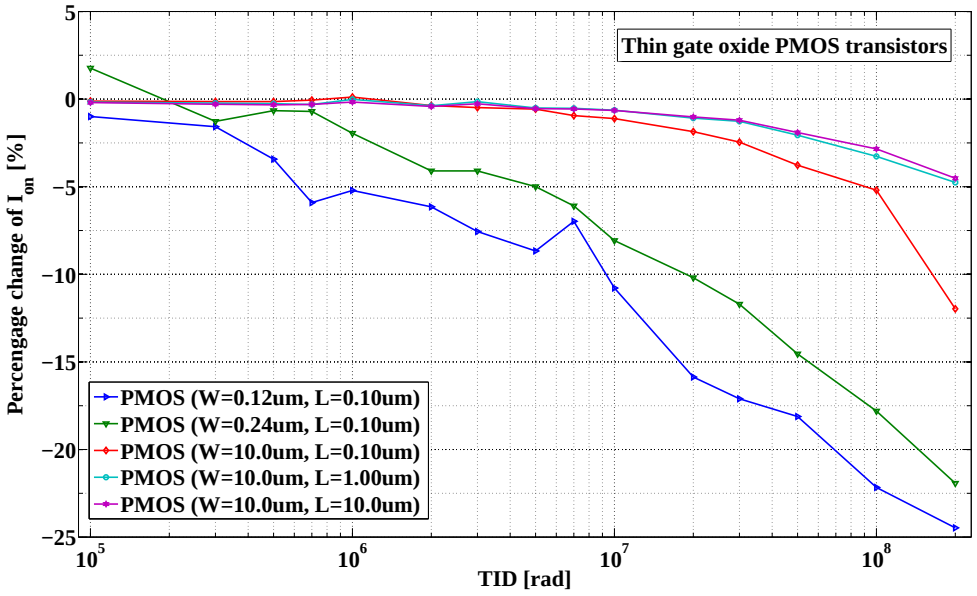

Figure 2.37: Percentage change of the on-current (I_{on}) with respect to its pre-irradiation value as a function of the TID for thin gate oxide, *p*-channel transistors manufactured in 90 nm technology node.

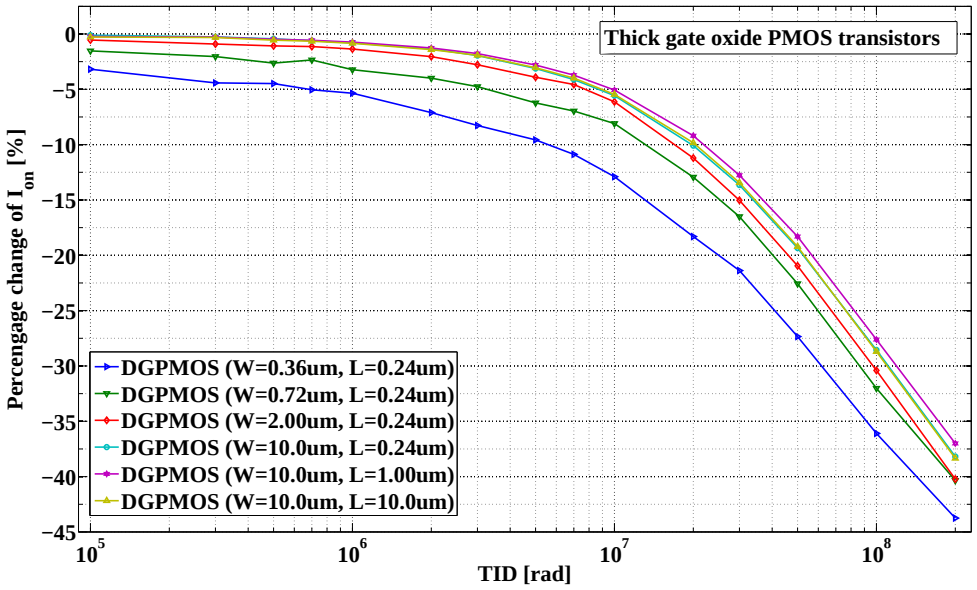

Figure 2.38: Percentage change of the on-current (I_{on}) with respect to its pre-irradiation value as a function of the TID for thick gate oxide, *p*-channel transistors manufactured in 90 nm technology node.

2.7 Conclusions

The results shown in the previous sections represent only a fraction of data collected from the TID3 (130 nm process) and TID90 (90 nm process) chip during the performed irradiation tests. In order to show only the main trends in the post-irradiation behaviour of the transistors, the regular-V_{th} thick and thin gate oxide FETs have been discussed here.

This chapter gives a brief overview of the pre- and post-irradiation technology performance. The presented results allow for a comparison of the 90 nm and the 130 nm CMOS processess. At the same time they show that the intrinsic radiation tolerance does not always scale down with the lithography node. The main conclusions coming from the collected data are following:

1. The voltage threshold shift is observed to be higher in the 90 nm CMOS process. For example, the maximum V_{th} shift measured for the minimum size thin gate oxide NFET is 15 mV higher than for a similar transistor laid out on TID3. The variation observed in the thick gate oxide NMOS transistors is much larger, up to 440 mV.

2. The leakage current in 90 nm CMOS is systematically higher by about one – two orders of magnitude in comparison with the 130 nm process. For instance, the leakage currents measured in the small thin and thick gate oxide transistors (90 nm)

are as high as 100 nA and 1 μA, respectively. However, one should note a very low initial (pre-irradiation) value of the leakage current at the level of pA for this process.

3. The radiation induced variation of the on-current is also more significant in the IBM 90 nm technology. In the small thin gate oxide NFET I_{on} rises by about 20 %, two times higher than in 130 nm. The largest change is observed at 100 Mrad for thick gate oxide PMOS transistors, maximally −30 % and −35 % in 130 nm and 90 nm, respectively.

The worse radiation tolerance of the transistors fabricated in the 90 nm process is caused by the fact that although the minimum channel length of a thin gate oxide transistor has been reduced from 130 nm down to 100 nm, the oxide thickness is reduced only from 2.2 nm to 2.1 nm. Additionally, the thickness of the STI has been increased from 0.35 μm to 0.43 μm, causing the significant increase in the leakage current. The measurements showed that the maximum leakage at 5 Mrad in a minimum size *n*-channel transistor is 5 nA and 30 nA for the 130 nm and 90 nm process, respectively. These numbers are significant if one considers a digital chip comprising hundreds of thousands of devices.

The better performance of 130 nm process manifests in lower threshold voltage shift, lower leakage current variations and smaller changes in on-current (on-resistance). However, comparing the pre-irradiation performance, the 90 nm process wins, mainly due to a very low leakage current.

In summary, one can formulate a set of rules which should be applied to future designs, in order to improve their radiation tolerance:

- Thin gate oxide transistors are much less susceptible to TID than thick gate oxide devices. Thick gate oxide devices should be avoided, unless they are absolutely required.

- All transistors with short channels (thin and thick gate oxide, *n*- and *p*-channel type) are affected more strongly by the Total Ionizing Dose effects. The undesirable threshold voltage shift and the leakage current can be significantly minimised by increasing the transistor channel length.

- Minimum size transistors of all kinds should be avoided due to their high sensitivity to TID.

- The ELTs are significantly less sensitive to radiation damage caused by TID. No increase in the leakage current is observed in any ELT at any dose. They however do still suffer from the threshold voltage shift and the variation of the on-current.

Chapter 3

Switched capacitor DC-DC converters

There are two different switched capacitor (SC) DC-DC converter designs presented in this dissertation; a step-up and a step-down converter. In general, a switched capacitor DC-DC step-up converter is a circuit providing the output voltage higher than the input voltage. The step-down SC DC-DC converter provides the output voltage lower than the input voltage.

The switched capacitor DC-DC converters are planned to be used in both alternative powering schemes currently being developed for the ATLAS Inner Detector after the High Luminosity Upgrade. In particular, switched capacitor DC-DC converters are critical components, which have to be implemented in the same technology as used in the front-end electronics, i.e. 130 nm CMOS as currently assumed.

In this chapter, the main types of power losses occurring in a switching MOSFET and the designs of two switched capacitor DC-DC converters are presented, together with results obtained from simulations and measurements.

3.1 Power losses in switching MOSFETs

A design of any type of a power converter is usually driven by one fundamental parameter, i.e. the power efficiency. Power efficiency, denoted by η_P[1], is the ratio between the available output power (P_{OUT}) and the total input power (P_{IN}), delivered to the circuitry (Eq. 3.1).

$$\eta_P = \frac{P_{OUT}}{P_{IN}} \tag{3.1}$$

In an ideal case, the total input power delivered to a circuit and the output power

[1]Power efficiency is here denoted by η_P to avoid the confusion with the pseudorapidity.

should be equal, resulting in a power efficiency of 100 %. This however is never the case due to power losses occurring in MOSFET switches and parasitic components. Figure 3.1 shows the topology of such a non-ideal DC-DC power converter.

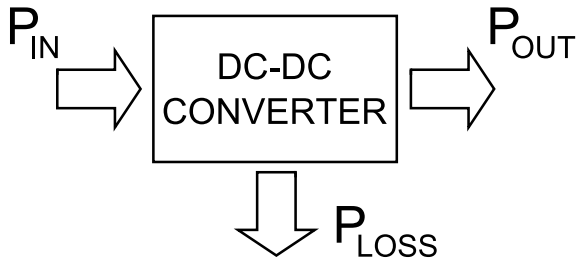

Figure 3.1: Power budget in a DC-DC converter.

Power loss (P_{LOSS}) is defined as a difference between the total input and total output power, and can be expressed as a function of power efficiency (Eq. 3.2). It is worth noting that power losses not only affect the efficiency of the converter, but they result in heat generation, which may degrade the overall reliability of the device.

$$P_{LOSS} = P_{IN} - P_{OUT} = P_{OUT}\left(\frac{1}{\eta_P} - 1\right) \tag{3.2}$$

Switching MOSFETs are usually the main source of power losses in power ASICs. Power loss occurs mainly due to the non-zero on-resistance and parasitic gate capacitance of the switch. One can distinguish the following types of losses [80] occurring in a switching MOS transistor:

- conduction loss; and
- switching loss.

3.1.1 Operation principle of the switched capacitor DC-DC step-up converter

A schematic diagram of a simple switched capacitor DC-DC converter [81], called charge pump, is shown in Fig. 3.2. In the simplest configuration the converter consists of a capacitor C_P and three switches (S_1, S_2, S_3). In order to introduce the load (R_L) into the circuitry, the charge pump must be modified by adding another switch (S_4) and the output capacitance (C_L). The switches are open or closed, depending on the clock phase and the capacitors play the role of charge reservoirs.

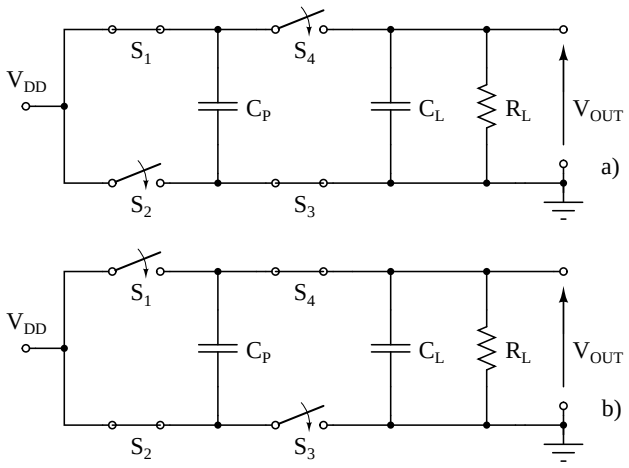

Figure 3.2: Schematic diagram of the voltage doubler with a resistive load in a charging (a) and discharging phase (b).

The switching period is divided into two phases. During the first phase (Fig. 3.2a), the capacitor C_P is connected between the input voltage and the ground, and charged $Q = V_{DD} \cdot C_P$. Then, during the second phase (Fig. 3.2b), the bottom plate of C_P is connected to V_{DD} and the top plate to the output. The capacitances C_P and C_L are in series and the maximum output voltage is equal to $2 \cdot V_{DD}$. The load current sunk by the load resistor is equal $I_{OUT} = V_{OUT}/R_L$.

One should also note that due to the continuous process of charging and discharging the capacitors voltage ripples occur at the output of the charge pump circuitry. However, by making the output capacitance sufficiently large one can reduce their amplitude to a negligible level in comparison with the mean value of the output voltage.

3.1.2 Operation principle of the switched capacitor DC-DC step-down converter

A schematic diagram of a simple two-stage switched capacitor DC-DC step-down converter [82] is shown in Fig. 3.3. The basic topology of such a converter comprises four series switches, denoted as S_1 through S_4, and two capacitances: a so-called flying (floating) capacitance C_X and a load capacitance C_L. The conversion ratio is defined as a relation between the maximum output voltage and input voltage. In many cases a conversion ratio higher than two is required. Such multistage converters are described in [83] and [84]. They allow obtaining the maximum output voltage being n-times lower than the input voltage. The presented converter has a conversion ratio of $1/2$.

The switching period is divided into two intervals: charging and discharging. During

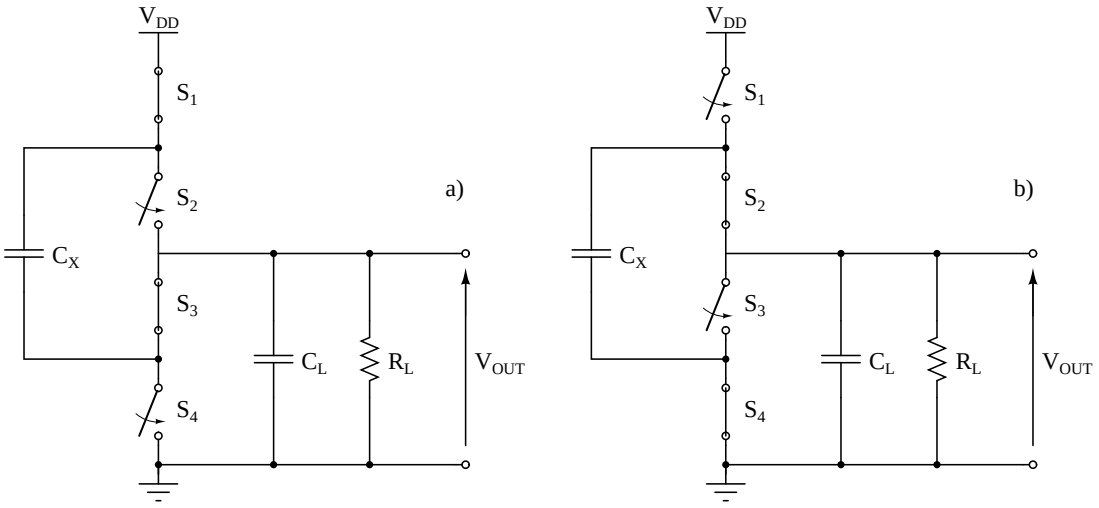

Figure 3.3: Schematic diagram of the switched capacitor DC-DC converter during the charging (a) and discharging interval (b).

the charging phase (Fig. 3.3a) switches S_1 and S_3 are closed and the flying capacitance is charged from the supply voltage. During the second, discharging phase (Fig. 3.3b), switches S_2 and S_4 are closed causing the flying capacitance C_X to be discharged into the load.

Due to the presence of the load the voltage ripples are observed at the output of the converter. The peak-to-peak value of ripples depends on the value of the output capacitance and can be significantly reduced by increasing C_L.

3.1.3 Conduction loss

The conduction loss in a MOSFET switch is due to its non-zero on-resistance (R_{on}). Assuming the MOSFET switch operation in an active region, where $V_{DS} < V_{GS} - V_{th}$, and using the small signal model of the transistor, R_{on} can be expressed as:

$$R_{on} \approx \frac{V_{DS}}{I_D} = \left[\frac{\mu \cdot C_{ox} \cdot W}{L} (V_{GS} - V_{th}) \right]^{-1}, \tag{3.3}$$

where V_{DS} is drain-to-source voltage, I_D is drain current, μ is carrier mobility, C_{ox} is gate capacitance per unit area, W/L is width to length ratio of the transistor and $V_{GS} - V_{th}$ is overdrive voltage. The above formula is an ideal model approximation. In fact, R_{on} is described by a more complex equation containing e.g. diffusion resistance of source and drain, resistance of contacts and metal lines. It is also temperature dependent.

According to Joule's first law, the conduction loss (P_R) in a MOSFET switch [80] is

given as:

$$P_R = I^2_{on(rms)} \cdot R_{on}, \tag{3.4}$$

where $I_{on(rms)}$ is an RMS value of the drain current.

In order to keep the conduction losses low the on-resistance has to be kept as low as possible. To achieve this, the designer should increase the W/L ratio of the transistor, but at the same time he must not forget to keep the overdrive voltage high. N-channel transistors would also be preferred over p-channel devices, due to higher carrier mobility.

Conduction loss due to a capacitor's parasitic Equivalent Series Resistance (ESR)

The non-zero on-resistance of the MOSFET switches is the main but not the only source of conduction losses in the circuitry. The conduction loss mechanism leads also to power loss in the parasitic Equivalent Series Resistance of the capacitors used in the design. Power P_E, given by Eq. 3.5, is lost due to a non negligible resistance in the external capacitors and metal wiring on the chip:

$$P_E = I^2_{OUT} \cdot R_{ESR}, \tag{3.5}$$

where I_{OUT} is the output (load) current and R_{ESR} is the sum of the parasitic equivalent series resistances of the capacitors C_X and C_L.

3.1.4 Switching loss

The power loss optimisation procedure is based mainly on tuning the W/L ratio of the MOSFET switches and the switching frequency.

There are several different mechanisms leading to power losses during MOSFET switching [85]. One can divide them into losses occurring due to charging and discharging of the gate capacitance and losses strictly dependent on the load.

Gate drive loss

The gate drive losses are caused by the charging and discharging of the gate capacitance in a MOSFET switch [86]. Figure 3.4 shows a schematic diagram of a circuit used for C_G estimation [87]. The resistance denoted as R_D is unavoidable and can be identified as a sum of the drain spread resistance and the resistance of the metal traces. Its value can vary between few tens of $\mathrm{m}\Omega$ up to a few Ω, depending on the layout and the size of the transistor.

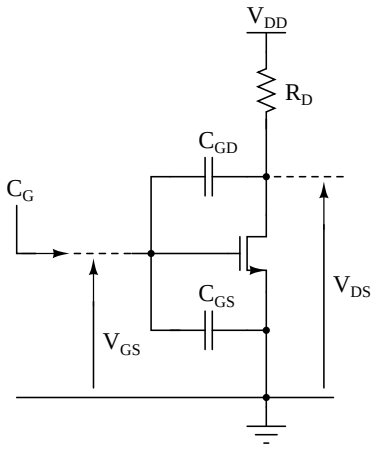

Figure 3.4: Schematic used to model the gate capacitance.

By definition, the energy stored in a capacitor is equal to the work done to charge it. Hence, assuming the switching frequency f_S, the expression for the power dissipated in order to charge the gate capacitance can be written as follows:

$$P_G = Q_G \cdot V_{DD} \cdot f_S = C_G \cdot V_{DD}^2 \cdot f_S, \tag{3.6}$$

where Q_G is the total charge accumulated on a gate capacitance C_G and V_{DD} is the driver supply voltage, which in this specific case is equal to V_{GS}. Equation 3.6 also shows that gate drive loss is frequency dependent. This becomes a reason for keeping the switching frequency low.

There are two main components of C_G, namely: gate-to-source capacitance (C_{GS}) and gate-to-drain capacitance (C_{DS}).

The simple circuit shown in Fig. 3.4 is a common source inverting amplifier. Hence, a total dynamic capacitance seen from the gate towards the drain of the transistor will be increased due to the Miller effect. An overall gate capacitance is expresses as a sum:

$$C_G(V_{GS}, V_{DS}) = C_{GS}(V_{GS}) + C_{GD}(V_{GD})[1 + A_v(V_{GS}, V_{DS})], \tag{3.7}$$

where $A_v(V_{GS}, V_{DS}) = -\partial V_{DS}/\partial V_{GS}$, is the gain of the amplifier.

Switching loss due to non-zero switching time of the MOSFET

The switching loss occurring due to turning the semiconductor switch on and off (P_S) should also be taken into account in the power budget of a switched capacitor DC-DC converter. It is proportional to switching frequency (f_S), switching time ($t_{SWon} + t_{SWoff}$),

source-to-drain voltage (V_{DS}) and drain current (I_D) [88]. This dependence is shown in Equation 3.8.

$$P_S = \frac{1}{2} V_{DS} \cdot I_D \cdot \left(t_{SWon} + t_{SWoff}\right) \cdot f_S \tag{3.8}$$

The above equation implies some important conclusions. Firstly, the switching loss is directly proportional to f_S. This means a better power efficiency of a converter could be obtained for lower switching frequencies. Secondly, power lost in the circuitry is dependent on the switching time, so the faster the rise and fall times the lower the switching loss. There is also an implicit dependence between the switching loss and the total gate capacitance. Big transistors used in order to minimise the conduction losses have large total gate capacitance (C_G). To charge this large capacitance one needs more time which according to Eq. 3.8 increases the switching loss.

Diode reverse-recovery loss

In this section the influence of the parasitic source/drain bulk junctions on the power efficiency of the converter is discussed.

This type of power loss occurs due to a source/drain bulk diode reverse-recovery mechanism [89] and can be described as follows. Before the diode moves from conduction to reverse-biased, minority charge, dependent on the forward current, stored in the junction must be removed. This can occur by passive removal through the recombination process. The remaining charge is removed actively through negative current flow. Hence, for a very short time (called the reverse recovery time or dead time) the diode remains forward-biased, causing power losses in the MOSFET.

The diode reverse-recovery losses (P_D) can sometimes significantly contribute to the power budget of converters switching large currents in short time intervals and can be expressed as follows:

$$P_D = 2 \cdot V_F \cdot I_D \cdot t_r \cdot f_S, \tag{3.9}$$

where V_F is the body diode forward voltage drop, I_D is the drain (output) current, t_r is the body diode conduction time and f_S is the switching frequency [90].

3.1.5 Power losses due to the shoot-through mechanism

One should also note that power loss in switching circuits may occur due to cross conduction or shoot-through [91]. Typically, a power converter contains MOSFET switches connected in series between the supply voltage and the ground. The shoot-through can be defined as the conduction state when both of these switches are fully

or partially turned on. The shoot-through can be efficiently minimized or avoided by introducing a dead time (both switches fully turned off) between the alternating clock signals used to drive the MOSFETs. The dead time must be sufficiently long in order to assure that the on-states of the switches never overlap. This can be achieved by introducing a non-overlapping clock generator into the converter circuit. The practical solution to this will be discussed later on.

3.1.6 Additional losses due to radiation effects in semiconductor devices

A power efficiency drop is expected to occur in switched capacitor DC-DC converters after irradiation due to a threshold voltage shift and increase of the leakage current. The leakage, however, can be minimised using special layout techniques, i.e. ELTs.

Both of the presented converters were laid out using only linear[2] geometry transistors. Despite that fact, some additional precautions were taken in order to minimise the leakage current and the transistor latch-up, a radiation induced effect which can be potentially destructive in power electronics. In particular, the transistors were protected by increasing the spacing between them and adding p^+ guardrings.

The thick gate oxide transistors are especially affected by the TID. The threshold voltage shift is higher resulting in a significant increase of the switch R_{on} (Eq. 3.3) and conduction losses.

Radiation induced increase of the leakage current changes the off-characteristic of the MOSFET switch. The increase of leakage current results in the decrease of the off-resistance and a loss of charge collected on capacitors.

3.2 Design of a switched capacitor DC-DC step-up converter in 130 nm CMOS technology

The presented switched capacitor DC-DC step-up converter has been designed taking into account the requirements for the analogue power supply for the front-end circuitry in the ABCN-13 chip. The topology of the converter is based on a classical concept of a charge pump [92]. As shown in [93] this concept can be implemented relatively easily in CMOS technology and very often is employed for generation of high voltage in battery powered devices. However, the typical required output currents in such circuits are limited. Thus,

[2]Transistors that have been laid out without using any dedicated radiation tolerant layout technique.

a very high power efficiency, beyond 90 %, can be obtained, but only in a low power application. The output current required to supply the front-end electronics in ABCN-13 is around 30 mA. This requirement implies that although the voltage doubler can be implemented on a silicon die, external Surface Mount Device (SMD) capacitors have to be used.

The design requirements for the switched capacitor DC-DC step-up converter are summarised in Table 3.1.

Table 3.1: The list of requirements for the design of the switched capacitor DC-DC step-up converter.

Parameter	Requirements
Input voltage	0.9 V
Output voltage	1.5 V–1.6 V
Maximum output voltage ripple	< 10 mV
Nominal output current	30 mA
Power efficiency	> 80 %

3.2.1 Architecture of the proposed switched capacitor DC-DC step-up converter

A schematic diagram of the developed voltage doubler [94] is shown in Fig. 3.5. The core of the circuitry consists of only six switches and four capacitors. In Fig. 3.5, one can find a pair of low-V_{th}, cross-coupled *n*-channel FETs (M_1, M_2) and four thick gate oxide *p*-channel FETs (M_3–M_6).

Three identical, external capacitances (C_{P1}, C_{P2} and C_L) are employed in the circuit. The fourth capacitance, $C_A = 1$ pF, is small enough to be integrated on the chip. This capacitance, together with transistors M_5 and M_6, forms an auxiliary charge pump, which is explained in Section 3.2.2.

The dimensions of the semiconductor switches M_1 through M_6 have been chosen after the optimisation process made with the Spectre circuit simulator. In order to assure the lowest possible on-resistance, transistors with minimum channel length were used while the width of the transistors was significantly increased. The dimensions of the used MOSFET switches are the following:

- W/L ratio of M_1 and M_2 is $980\,\mu\text{m}/0.15\,\mu\text{m}$;

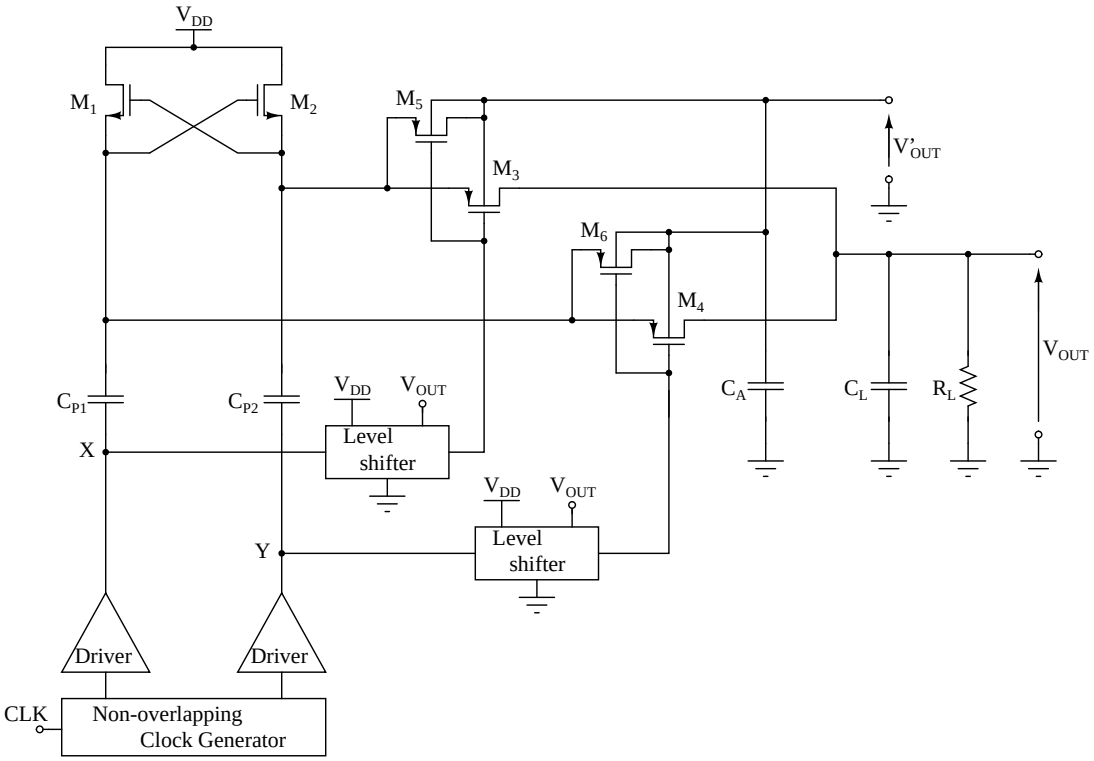

Figure 3.5: A schematic diagram of the proposed voltage doubler circuitry.

- W/L ratio of M_3 and M_4 is $2000\,\mu m/0.24\,\mu m$; and
- W/L ratio of M_5 and M_6 is $10\,\mu m/0.24\,\mu m$.

The three external SMD capacitors, of 470 nF, each are used as C_{P1}, C_{P2} and C_L. In order to minimise the conduction losses, capacitors with low ESR are required. The capacitors serve as charge reservoirs hence the required capacitance values depend on the load current and the switching frequency. The 470 nF capacitors offer a good compromise between a large capacitance value and a relatively small package size, which is 0603 ($0.61\,mm \times 0.30\,mm$). Also, capacitors of higher values can be used in the future if they are available in packages, like 0603 or smaller. However, some minor changes in the drivers' design would be required in order to assure good driving capability. The capacitor packaging is one of the main constraints and is related to limitations concerning material budget of the detector module.

Operation of the proposed voltage doubler

The voltage conversion method used in the proposed converter topology is exactly the same as the one presented in Section 3.1.1. A big advantage of the proposed architecture

is that there are two charging and discharging phases during each clock period. If the clock signal is high at "X" and low at "Y" (Fig. 3.5), then the transistors M_2 and M_4 are on, while M_1 and M_3 are off. A simplified diagram illustrating this case is shown in Fig. 3.6a. The top plate of C_{P2} is connected to the supply voltage and the capacitor is charged. At the same time, C_{P1} and C_L are connected in parallel. The bottom plate of C_{P1} is at a high potential and the charge stored there in the previous phase is now moved into the load. Fig. 3.6b shows the second phase of operation. Now transistors M_1 and M_3 are turned on and M_2 and M_4 are off. The top plate of C_{P1} is charged from V_{DD} and C_{P2} is connected in parallel with the load.

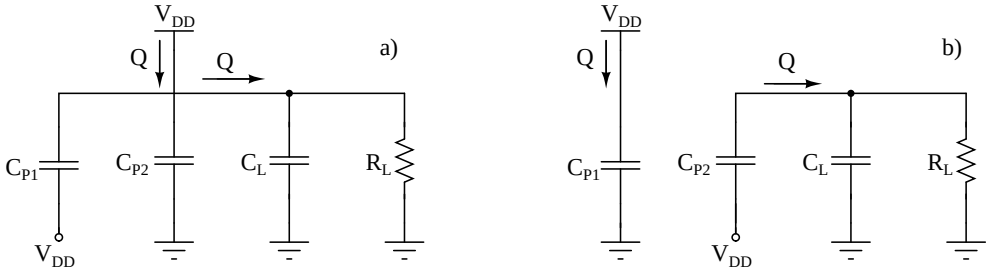

Figure 3.6: The principle of operation of the voltage conversion in the proposed voltage doubler.

3.2.2 Auxiliary circuitry used in the design

The core of the voltage doubler consisting of transistors (M_1 through M_4) and capacitors (C_{P1}, C_{P2} and C_L) can be considered as a stand-alone circuit, assuming that external non-overlapping clock signals are applied. However, four auxiliary building blocks are added to the core of the charge pump in order to increase its power efficiency, namely an auxiliary charge pump used for switch biasing, level shifters, buffers and a non-overlapping clock generator.

Auxiliary charge pump

The auxiliary charge pump implemented in the presented design consists of p-type transistors M_5, M_6 and a capacitor C_A. It also shares M_1, M_2 and C_{P1}, C_{P2} with the core of the main power converter (Fig. 3.5).

One should note that the auxiliary pump is capacitively loaded, so its power efficiency is expected to be higher than the power efficiency of the main voltage doubler. It can produce the output voltage V'_{OUT}, a few tens of mV higher than V_{OUT}. The circuit is used to tie the n-wells with serial PMOS switches (M_4 and M_3) to V'_{OUT} in order to avoid

switching on the parasitic vertical bipolar (*pnp*) transistor. This solution assures that all the *pn* junctions between the *n*-well and the drain / source of M_4 and M_3 are reverse biased during the voltage doubler operation. [93].

Level shifters

One of the critical aspects of the design is the driving of the large *p*-channel serial switches M_3 and M_4. The maximum available input voltage to the circuit is 0.9 V. Taking into account that the threshold voltage of the MOSFET transistor is around 0.5 V the overdrive voltage is too small to make the switches fully conductive. This results in a relatively high on-resistance. As a consequence, the conduction losses would be high and the power efficiency would drop.

A significant improvement can be obtained by introducing a level shifter circuit [95] into the design. Such a circuit shifts the high level of the clock signal from 0.9 V determined by the input voltage up to its doubled value obtained from the output of the charge pump. This clock signal applied on the gates of the serial PMOS switches (M_3 and M_4 in Fig. 3.5) increases the overdrive voltage and decreases the on-resistance.

A schematic diagram of the proposed level shifter is shown in Fig. 3.7. The circuit is supplied from two power domains. The thick oxide transistors M_1 through M_6 are supplied from the output of the voltage doubler with V_{OUT}. Only the inverter comprises of thin gate oxide transistors supplied with a voltage of 0.9 V.

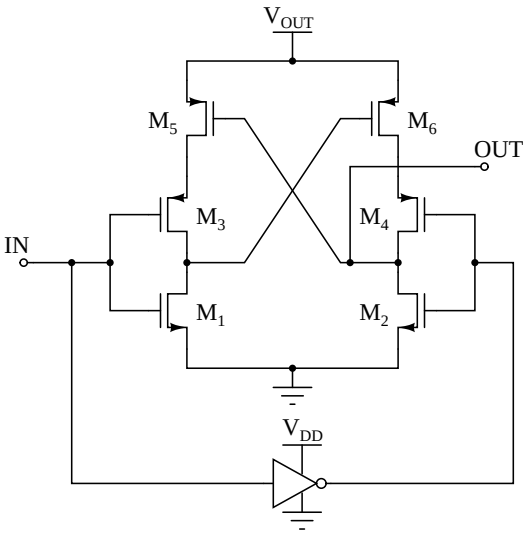

Figure 3.7: Schematic diagram of a level shifter used in a design of the step-up converter.

The operation principle of the level shifter is simple. For the input clock signal in high

state the transistors M_1, M_4 are switched on and M_2, M_3 are switched off. The drain of M_1 is pulled down to the ground, which turns on the *p*-channel transistor M_6 and turns off M_5. The output of the level shifter (the drain of transistor M_2) is now pulled up to the supply voltage V_{OUT}. Similarly, when the input signal is low, it turns off M_1, M_4 and turns on M_2, M_3. The drain of M_2 (the output of the level shifter) is pulled down to the ground.

The choice for transistor sizing in the level shifter is not very critical. However, the circuit must be able to drive the big *p*-channel serial switches of the voltage doubler. Based on Spectre simulations the minimum channel length $L = 0.24\,\mu\text{m}$ for all the transistors and the widths have been selected as follows: $W_{M1-M4} = 45\,\mu\text{m}$ and $W_{M5-M6} = 35\,\mu\text{m}$. The transistors used in the inverter have $W/L = 10\,\mu\text{m}/0.12\,\mu\text{m}$ and $W/L = 5\,\mu\text{m}/0.12\,\mu\text{m}$ for PMOS and NMOS, respectively.

Buffers and non-overlapping clock generator

The requirement for low conduction loss imposes the use of large MOSFET switches. In order to switch them efficiently in a relatively short time, drivers of sufficient driving capability are required. Each driver used in the charge pump circuitry consists of a chain of seven scaled inverters, built of minimum channel length thin gate oxide transistors. The last inverter in a chain employs a *p*-channel transistor 1680 µm wide and an *n*-channel transistor 690 µm wide.

The undesirable effect of shoot-through (Section 3.1.5) can be minimised by introducing a dead time between the clock signals. This means that the rising edge of the clock signal applied at the input of one driver (Fig. 3.5) is well separated from the clock signal applied at the input of the second driver. As a result the transistors driven by these buffers can not be switched on at the same time. The clock signal separation is realised by the non-overlapping clock generator. Its schematic diagram is shown in Fig. 3.8 [96].

The required separation of the clock signals is achieved by introducing a delay into the circuit. The delay line consists of a classical CMOS inverter, a capacitor C_D and an inverted Schmitt trigger.

The capacitor C_D is used to increase the fall and the rise time of the clock signal seen at the input of the second stage. The value of C_D used in the delay line was chosen to be 1 pF. The Schmitt trigger is used to recover clock signals with good quality. For instance, the design was made assuming 2 ns rise time of an external clock. The rise time of the same signal at the output of the first delay stage is 16.4 ns and at the output from the clock generator it is reduced to 3.8 ns. The presented solution allows the separation of the clock signal edges by 10.3 ns.

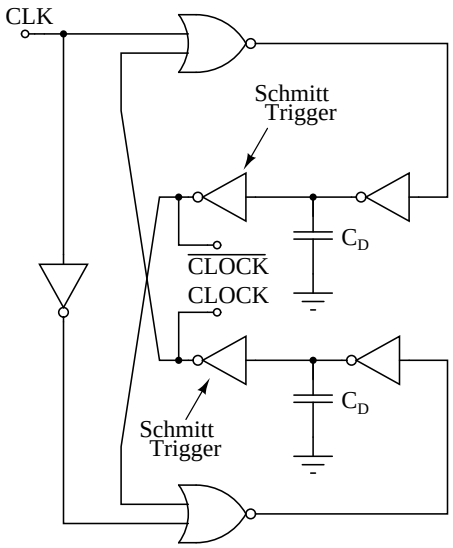

Figure 3.8: Schematic diagram of the non-overlapping clock generator.

3.2.3 Performance of the step-up converter

In order to estimate the power efficiency of the converter one has to extract the value of P_{OUT} and P_{IN}. This can be done easily by analysing the voltage and current waveforms obtained from the transient simulation.

Simulation results of the step-up converter

The behaviour of the presented switched capacitor DC-DC step-up converter was simulated using Cadence Virtuoso Spectre Circuit Simulator[3].

Figure 3.9 shows the observed input and output signals. The input voltage is ramped up to 0.9 V in 50 µs. The output voltage reaches its nominal value of 1.58 V after 80 µs. The circuit was optimised to make the unavoidable output voltage ripples small, around 5 mV peak-to-peak. A power efficiency calculated for the nominal output current of 30 mA was as high as 85 %. The presented results were obtained for the external capacitor's ESR value of 10 mΩ.

Additionally, in order to investigate the behaviour of the converter with wire bonding, the parasitic inductance was introduced into the simulation cell. It was observed that adding a 0.5 nH inductance results in voltage spikes up to 0.93 V peak-to-peak at the input and 1.68 V at the output of the circuitry. The observed voltage signals are shown in Fig. 3.10 and Fig. 3.11.

[3]Spectre Circuit Simulator is a SPICE-class circuit simulator, providing fast and accurate simulation for analogue, radio frequency (RF) and mixed-signal circuits [97].

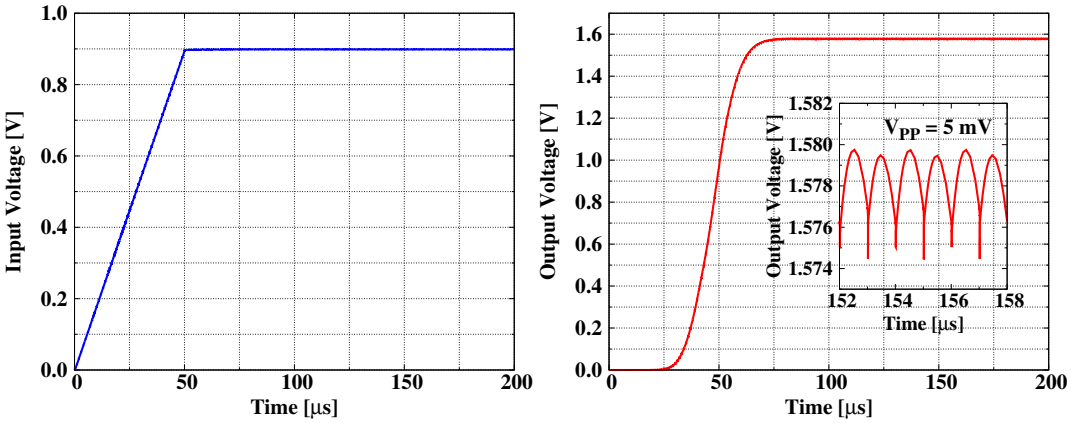

Figure 3.9: Simulated time response of the switched capacitor DC-DC step-up converter.

The mechanism of the voltage spikes creation is described directly from Eq. 3.10:

$$v(t) = L\frac{\mathrm{d}\,i(t)}{\mathrm{d}t}, \tag{3.10}$$

where L is the self inductance, $v(t)$ denotes the voltage and $i(t)$ denotes the current. Hence, the voltage spikes are unavoidable if the bond wires have a non-zero inductance. To reduce this issue to an negligible level one can use another assembly technique, for example flip chip bonding, which results in much lower inductance of the connections. It is worth mentioning that the voltage spikes do not affect the power efficiency since they are symmetric.

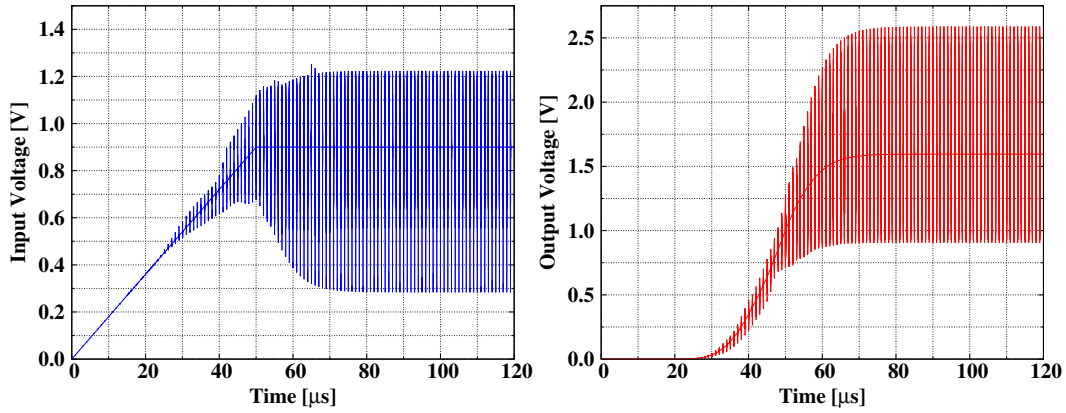

Figure 3.10: Simulated time response of the switched capacitor DC-DC step-up converter, including all package components.

A very important parameter for each power converter design is the switching

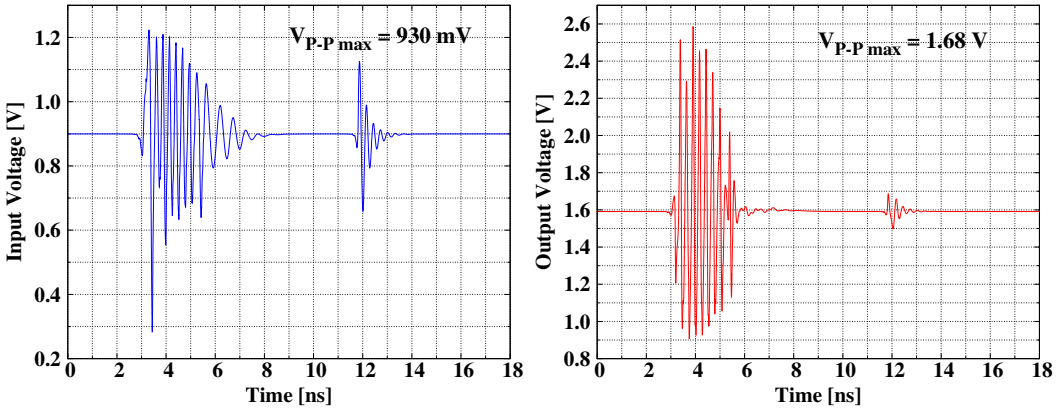

Figure 3.11: Voltage spikes observed at the input (left) and output (right) of the switched capacitor DC-DC step-up converter.

frequency. It has already been shown that the switching frequency influences the power efficiency through switching losses in the MOSFET switches. It also determines the peak-to-peak value of the output voltage ripples. Figure 3.12 shows the dependence between the switching frequency, the output voltage, power efficiency and the peak-to-peak value of the voltage ripples. In order to satisfy the design specification presented in Table 3.1, the switching frequency in the switched capacitor DC-DC step-up converter was chosen to be 500 kHz. This choice guarantees the power efficiency for the nominal current at the level of 85 %, the maximum output voltage of 1.58 V and the peak-to-peak value of the output voltage ripples as high as 5 mV for the output capacitance of 470 nF.

The transfer and output characteristics are presented in Fig. 3.13 and Fig. 3.14, respectively. The transfer characteristics were obtained by running several transient analyses with different input (supply) voltages, from 0.7 V to 1.4 V. The switching frequency was fixed at 500 kHz. Assuming that there were no losses, the characteristics should be $V_{OUT} = 2V_{IN}$. For the presented converter, the trend line is given by: $V_{OUT} = 2.0059V_{IN} - 0.2363$. The power efficiency increases for higher input voltages mainly due to better driving capability of the big PMOS switches, reaching 87 % for input voltage of 1.4 V.

The output characteristics obtained for the switching frequency of 500 kHz and supply voltage of 0.9 V show (Fig. 3.14) how the load influences the output voltage and the power efficiency. The step-up converter was designed and optimised for an output current as high as 30 mA and it was assumed that the power consumption in the analogue front-end circuitry will be constant in time. Nevertheless, some fluctuations in current consumption are unavoidable.

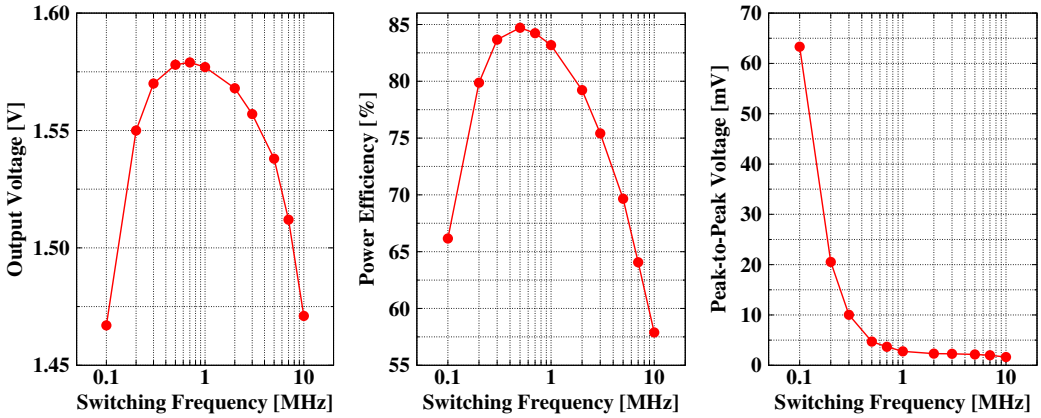

Figure 3.12: Output voltage, power efficiency and output voltage ripples as a function of switching frequency simulated for the SC DC-DC step-up converter.

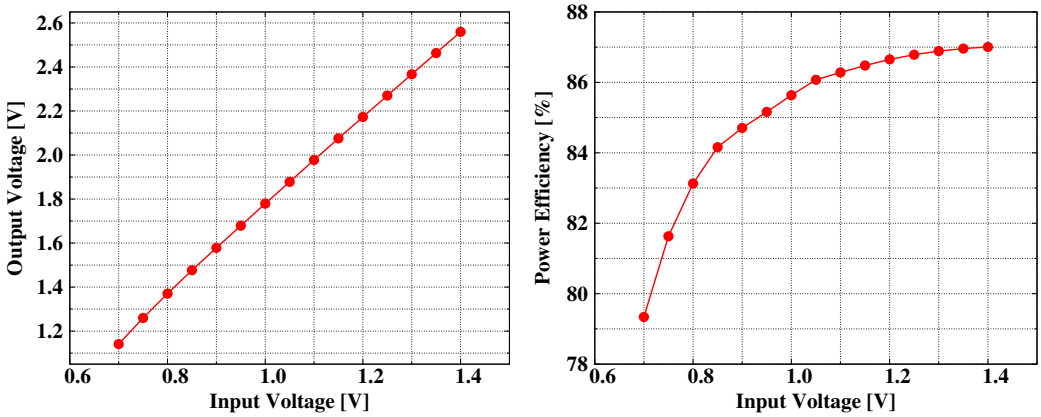

Figure 3.13: Simulated transfer characteristics of the step-up converter, the output voltage (left) and the power efficiency (right) as a function of the input voltage.

Test results of the step-up converters

The step-up converter is supplied with 0.9 V. Additionally, the voltage of 3.3 V is required by the electrostatic discharge protection circuits and the digital interfaces. Inside the chip the high and low level of the clock signal are 0.9 V and 0 V, respectively. A constant voltage is provided by the Agilent E3631A power supply. A HP8110A clock generator provides the clock signal of 500 kHz. An Agilent Infiniium 54831B, 600 MHz 4 channel oscilloscope is used to read out input and output voltage signals. A Tektronix TCPA300 current probe is used to measure the currents.

The chip with the prototypes is wire bonded in the middle of the test PCB, shown in Fig. 3.15. The bond wires are roughly 3 mm long. All the external, SMD components

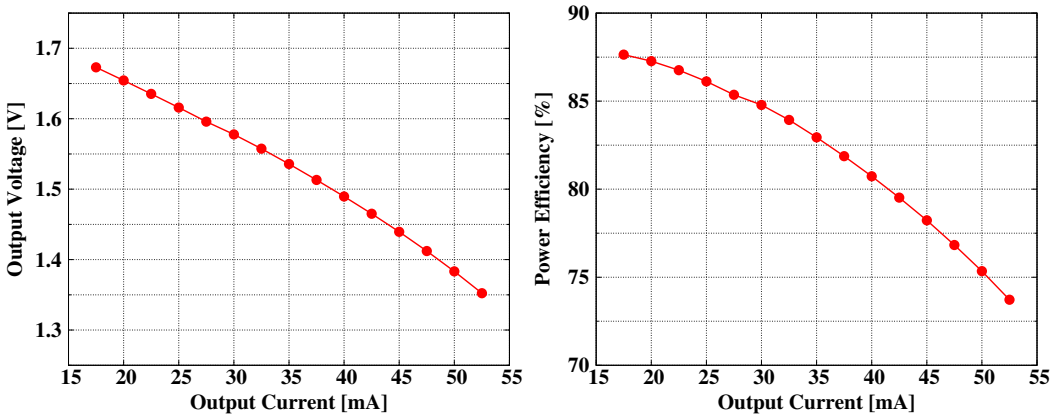

Figure 3.14: Simulated output characteristics of the step-up converter, the output voltage (left) and the power efficiency (right) as a function of the output current.

(capacitors, resistors, connectors) are soldered on the bottom side of the board to allow the access for the wedge bonder.

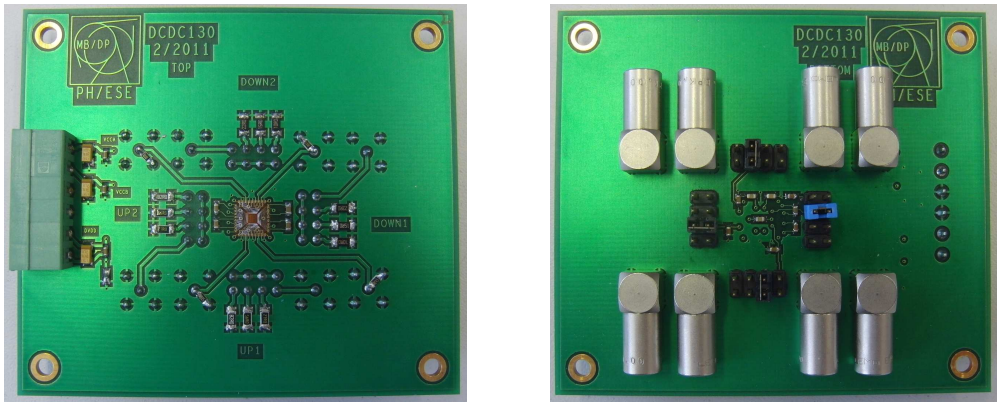

Figure 3.15: PCB with the prototype chip used for tests of the switched capacitor DC-DC converters.

Both presented converters use external SMD components, capacitors and resistors. The step-up converter requires three 470 nF low-ESR capacitors. Resistors of 27 Ω, 56 Ω and 82 Ω are used to emulate the load of the converter. For nominal output voltage of around 1.55 V these resistors correspond to load currents of 57 mA, 28 mA, 19 mA, respectively.

Additionally, in order to provide good filtering of the input voltage, three decoupling capacitors of 10 nF, 470 nF and 10 µF connected between the supply line and the ground are mounted on the PCB.

Figure 3.16 shows the output voltage waveform from the step-up converter measured for the switching frequency of 500 kHz. The calculated RMS values of the output voltage

and current are $V_{OUTrms} = 1.529\,\text{V}$ and $I_{OUTrms} = 27.88\,\text{mA}$, respectively. The average input current (I_{INavg}) is as high as $55.81\,\text{mA}$ and gives the power efficiency of 85 %, assuming constant voltage of $V_{INavg} = 0.898\,\text{V}$ from the power supply.

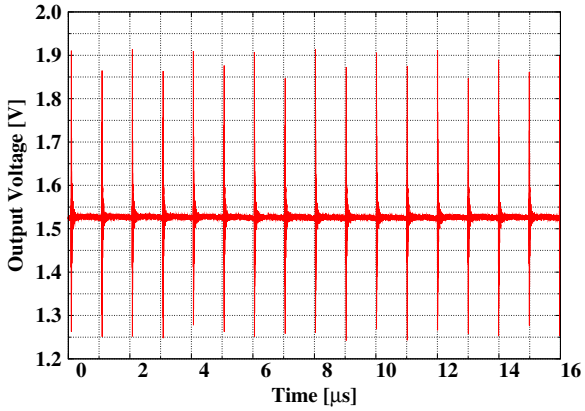

Figure 3.16: Measured transient response of the step-up converter.

The voltage spikes (Fig. 3.17) are present, just like it was foreseen in simulations. A measured maximum peak-to-peak value of such a voltage spike is 580 mV. The length of the bond wires is around $3-4\,\text{mm}$, hence the effective inductance is around $0.4-0.5\,\text{nH}$ for the converter connected with 8 V_{DD} bond wires interleaved with 8 ground bond wires. A maximum peak-to-peak value of the voltage spike obtained from simulation is roughly three times higher.

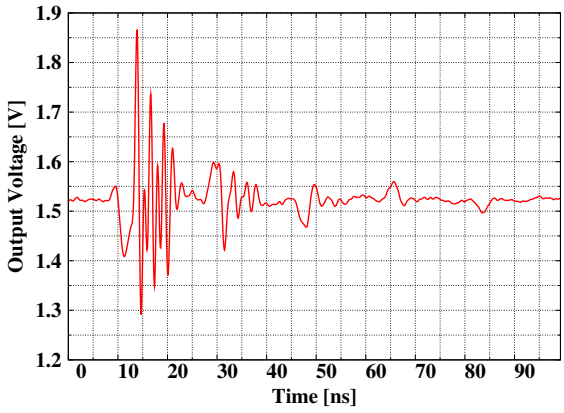

Figure 3.17: Voltage spike measured at the output of the step-up converter.

In order to properly evaluate the circuit, it is important to check how the switching frequency, input voltage and output current influence the output voltage and the power efficiency. Hence, three different characteristics (frequency, transfer and output) have been measured.

Figure 3.18 shows the measured frequency characteristic of two SC DC-DC step-up converters from the same chip. The measurement confirms that the optimum switching frequency is around 500 kHz with a relatively broad plateau up to 1 MHz. The power efficiency drops very quickly for the frequencies above 1 MHz due to the increase of switching losses.

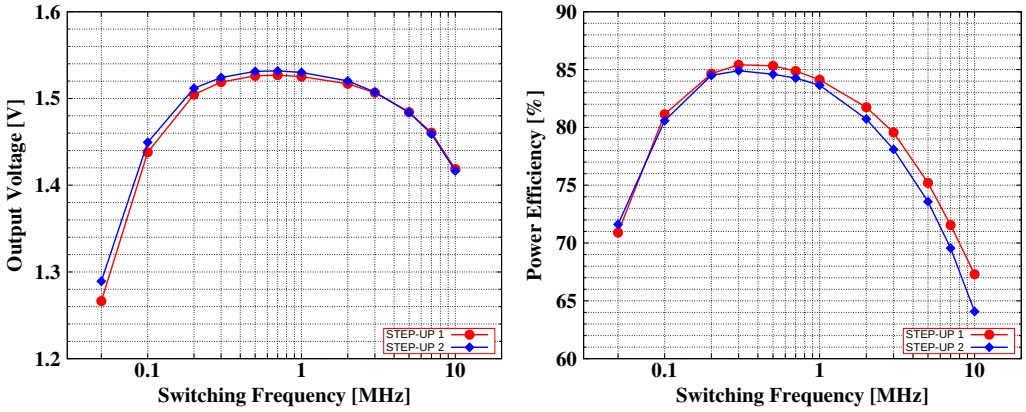

Figure 3.18: Measured values of the output voltage and the power efficiency as a function of the switching frequency for two step-up converters.

The transfer characteristics are shown in Fig. 3.19. They prove that the converter is linear in a wide range of input voltages. In an ideal case the input voltage would be doubled, but due to a non-zero output resistance the maximum output voltage is always lower. For the nominal input voltage the voltage measured at the output is 1.53 V. One should also note that the power efficiency increases together with the input voltage.

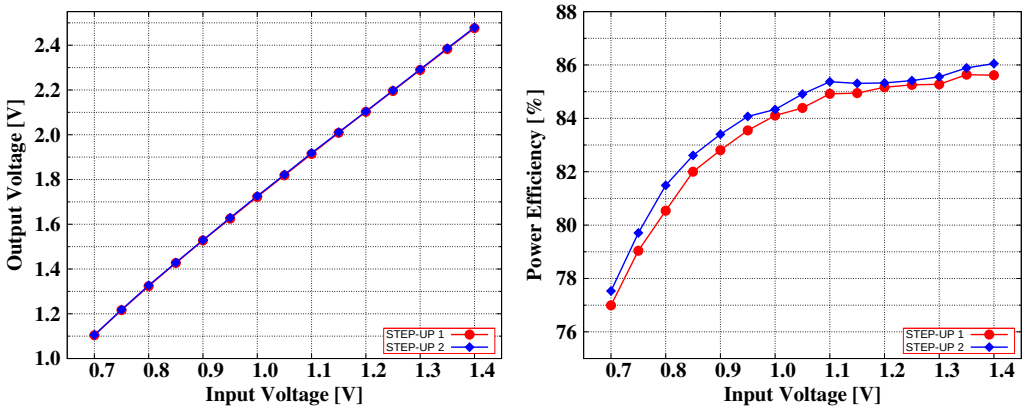

Figure 3.19: Measured transfer characteristics of two step-up converters, the output voltage (left) and the power efficiency (right) as a function of the input voltage.

The output characteristics (Fig. 3.20) describe how the load influences the output

voltage and the power efficiency. Although the power consumption in the ABCN-13 analogue read-out channel is assumed to be constant, it is crucial to keep the output voltage at a level which allows its regulation by the linear regulator even if the current consumption increases for any reason. It is obvious that an increase of the load current will increase the conduction losses in the switches and will affect the maximum output voltage and the power efficiency. The output characteristic (Fig. 3.20) shows that an increase of the load by 30 % allows the power efficiency to be kept at a reasonable level of approximately 70 %. However, to have the possibility of voltage filtering done by a linear voltage regulator, the output current must not exceed 42 mA.

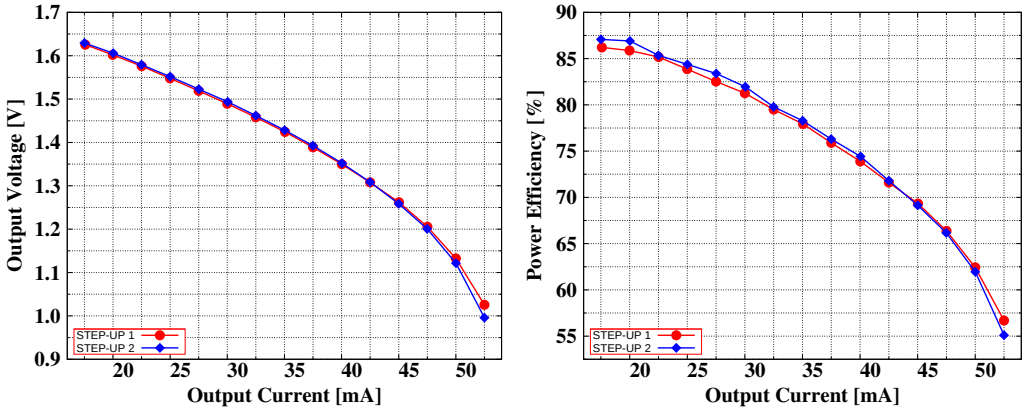

Figure 3.20: Measured output characteristics of two step-up converters, the output voltage (left) and the power efficiency (right) as a function of the output current.

The output characteristic can be also used to evaluate the output impedance of the step-up converter, which is extracted as the slope of the $V_{OUT}\,(I_{OUT})$ curve. The difference between simulated and measured value is big, 8.1 Ω and 12.1 Ω, respectively. Such a high resistance can not only be caused by the parasitic resistance of the bond wires nor the metal lines on the chip and the test board. In the worst case, its contribution should not exceed a few hundreds of mΩ. The simulations showed that the threshold voltage of a large PMOS switch used in the design is typically $V_{th} = -522$ mV, but it can change between -447 mV and -577 mV due to process variations. This effect could partially explain the increase of the output resistance of the converter, which strongly depends on the threshold voltage.

Post-irradiation test results of the step-up converter

The irradiation was performed, using CERN's in-house X-ray generator presented in Section 2.3, for the tube current of 50 mA and power supply voltage of 50 kV. At these

conditions and at a given geometry, the dose rate of 68.65 rad/s was obtained. The chips bonded on a PCB were irradiated up to a TID of 200 Mrad after approximately 80 hours at room temperature. After the irradiation they were annealed for 168 hours in an oven at a temperature of 100 °C according to the Standard Tests Procedures, ESA/SCC 2900 [98] and MIL STD 883 1019.5 [99].

From the plots shown in Fig. 3.21 one can see that the measured output voltage and power efficiency do not change up to a TID of about 10 Mrad. For higher doses, a rapid drop of the output voltage and the power efficiency can be observed. The calculated relative decrease of output voltage and efficiency is less than 8 % and 10 %, respectively. This test was made for a resistive load of 56 Ω, connected to the output of the converter.

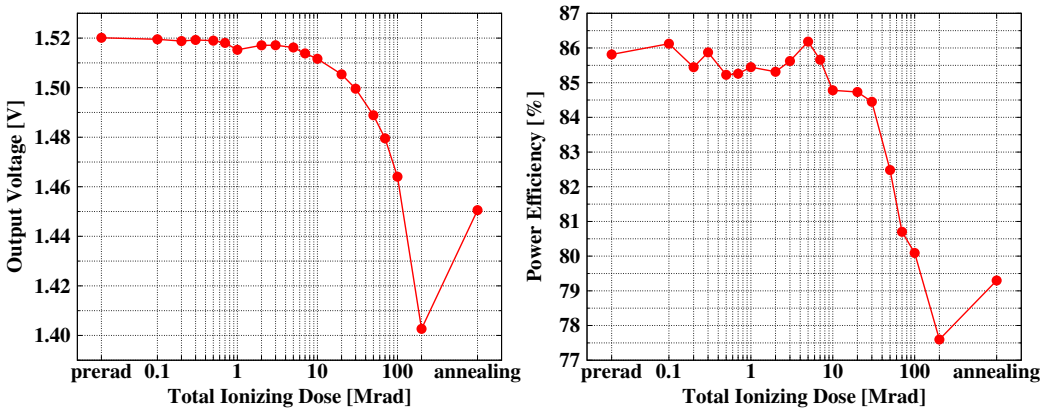

Figure 3.21: Measured value of the output voltage (left) and the power efficiency (right) for different TIDs.

One should note that according to the current plans, the step-up converter in the serial powering scheme will be followed by a linear regulator in order to obtain a clean supply voltage for the analogue circuitry on the front-end chip. The regulator requires at least 100 mV of dropout voltage to keep the pass transistor in saturation. Hence, in order to keep the analogue voltage at a constant level of 1.2 V the output voltage from the step-up converter must be higher than 1.3 V.

The annealing only partially restores the performance of the step-up converter. After one week in 100 °C the maximum output voltage increased up to 1.45 V and the power efficiency reached 79 %.

Figure 3.22 shows the evolution of the output characteristics of the SC DC-DC step-up converter. The red curve represents the data collected before the irradiation and the blue curve, after the chip irradiation up to 200 Mrad. The green curve denotes the output characteristic of the converter measured after annealing.

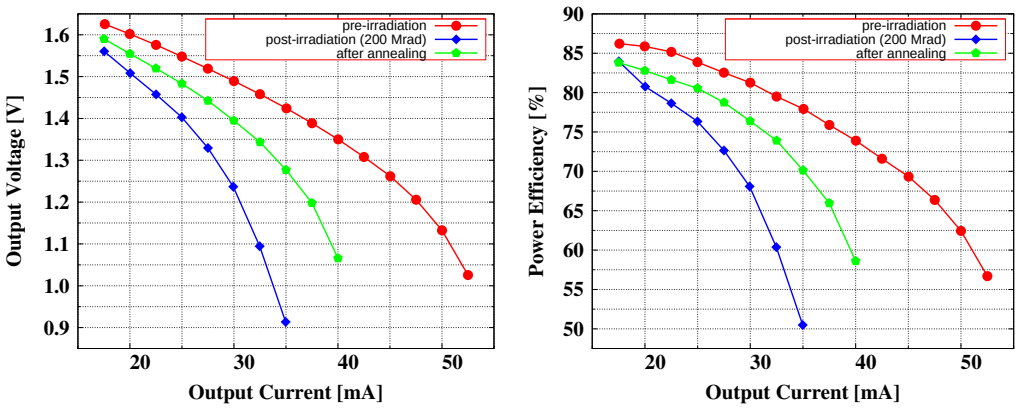

Figure 3.22: Measured output characteristics of the SC DC-DC step-up converter before irradiation (red line), after irradiation (blue line) and after annealing (green line).

A degradation of the output resistance of the converter after the irradiation is clearly visible. The output resistance has been extracted for the nominal output current of 30 mA. A fourfold increase of the output resistance, comparing to the pre-irradiation measurement, has been observed after the circuit irradiation up to a TID of 200 Mrad. The post-irradiation value of R_{OUT} is as high as 47.2 Ω. The output voltage for the nominal analogue current of 30 mA measured in the irradiated converter is around 1.25 V, so 50 mV lower than allowable minimum.

After the chip was annealed for one week at the temperature of 100 °C the output resistance of the step-up converter was measured again. The measured value of the output resistance after the annealing is 19.8 Ω.

Such degradation of the converter performance occurs due to the fact that a pair of thick gate oxide PFET switches has been used. As shown in Chapter 2, the threshold voltage in the narrow *p*-channel transistors shifts significantly, due to the positive charge deposition in the gate oxide occurring during irradiation. It was shown that the observed V_{th}-shift is more significant in case of narrow devices and affects the on-resistance of the switch (Eq. 3.3) leading to the increase of conduction losses.

Another serious radiation induced effect which causes the degradation of the circuitry performance is the increase of the leakage current. A positive charge trapped in the STI leads to the creation of a parasitic channel and parasitic current flow between the source and drain, even when the transistor is turned off. This causes a decrease of the power efficiency due to continuous discharging of the capacitors.

There are several ways to improve the performance of the presented converter after irradiation. First, in order to reduce the conduction losses occurring due to the

increase of the on-resistance during irradiation, one could consider making the MOS switches sufficiently bigger. Thus, even after irradiation their on-resistance will remain at a sufficiently low level. This of course would require some modifications to the design of the drivers.

The power inverters that are used to drive the large MOS switched are optimised and balanced assuming the pre-irradiation values of the threshold voltage. The threshold voltage however shifts with the TID. Hence, it would be possible to tune the size of these inverters so their performance is satisfactory also after irradiation.

The power loss due to the leakage current in the NMOS transistors can be effectively reduced through the use Enclosed Layout Transistors instead of devices with the standard, linear geometry.

3.3 Switched capacitor DC-DC step-down converter

Switched capacitor DC-DC step-down converters are assumed to be used in the parallel powering scheme employing a DC-DC conversion technique. In such a scheme, separate step-down converters will supply the analogue and digital circuitry of the front-end chip. The converters will be implemented on the ABCN-13 in order to provide voltages of 1.2 V and 0.9 V. The requirements concerning the load current are the following: around 30 mA for analogue and around 60 mA for digital circuit. The design has been optimised for the digital power supply, assuming that the performance of the device used for the analogue power supply will be better due to a smaller load.

3.4 Design of a switched capacitor DC-DC step-down converter in 130 nm CMOS technology

The topology of the presented switched capacitor DC-DC converter is based on the architecture of the power converters discussed in [100] and [101]. The converter has been designed and manufactured in the same technology (IBM CMOS 130 nm) as currently assumed for the upgrade of the ID electronics.

A schematic diagram of the proposed switched capacitor DC-DC step down converter is shown in Fig. 3.23. The converter was designed to obtain 0.9 V of output voltage from the voltage supply of 1.9 V and optimised to achieve the highest possible power efficiency for a nominal load of 60 mA.

All the transistors used in the design are thick gate oxide ($t_{ox} = 5.2$ nm) devices,

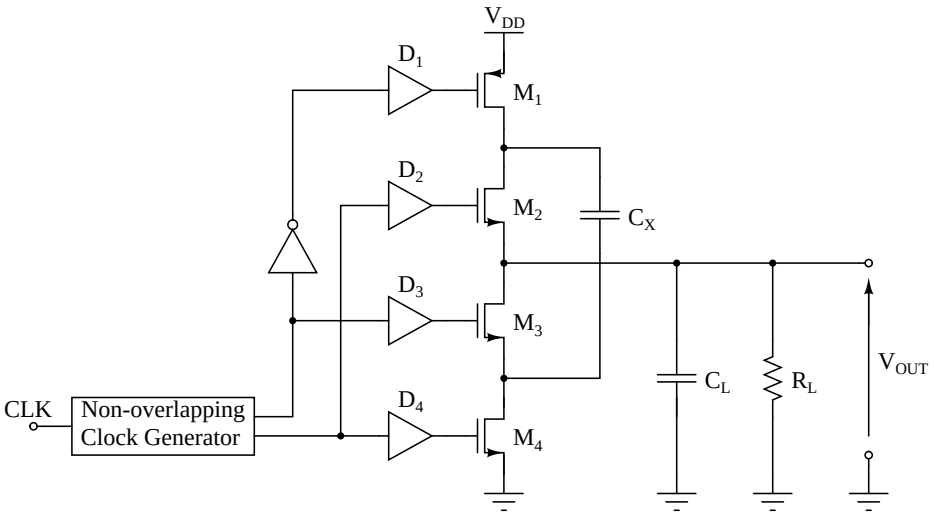

Figure 3.23: Schematic diagram of a practical implementation of the switched capacitor DC-DC step-down converter.

otherwise operation with voltages higher than 1.7 V would not be possible. The transistor M_1 is a *p*-channel device, because it can be easily driven. The transistors M_2 through M_4 are *n*-channel devices. The W/L ratios of all switches are summarised in Table 3.2. These values were chosen, based on Spectre simulations, to minimise the power losses.

Table 3.2: MOS switches used in the design of switched capacitor DC-DC step-down converter.

Switch	Switch dimensions (W/L)
M_1	28.2 mm / 0.24 µm
M_2	18.0 mm / 0.30 µm
M_3	18.0 mm / 0.30 µm
M_4	6.0 mm / 0.30 µm

The IBM 130 nm CMOS technology offers triple-well devices providing *n*-channel transistors within a well, isolating them from the substrate. They are used in the design in order to avoid the body effect [102], leading to an increase of the threshold voltage. It is important to remember that the value of V_{th} depends on the source-to-bulk voltage (V_{SB}), and the on-resistance, according to Eq. 3.3, depends on the overdrive voltage ($V_{GS} - V_{th}$).

The triple-well NFET allows a short circuit between the source and local *p*-substrate, making $V_{SB} = 0$. The triple-well transistor also provides better isolation from the global *p*-substrate, thereby reducing the amount of charge injected into the substrate.

The values of the external SMD capacitors have been chosen as $C_X = 1.0\,\mu\text{F}$ and $C_L = 0.2\,\mu\text{F}$. Simulations showed that the best converter performance was obtained for $C_X/C_L = 5$.

3.4.1 Auxiliary circuitry used in the design

In order to achieve the desired performance of the switched capacitor DC-DC step-down converter, some auxiliary circuitry is needed. The most crucial for the power efficiency is proper driving of the large MOSFET switches. Hence, dedicated drivers must be developed. A non-overlapping clock generator is also needed to minimise the power losses occurring due to cross conduction. A sufficiently long dead time between the alternate clock signals should be implemented to assure that the on-states of the switches do not overlap under any conditions.

Non-overlapping drivers

The MOSFET switches used in a converter design are large and they can not be driven directly from the internal clock generator. A chain of scaled inverters would be the simplest implementation. However, in this case to improve the performance more sophisticated topology [103] of a driver, shown in Fig. 3.24, is used. This driver consists of two chains of scaled inverters. Each chain drives a single big transistor of the output stage. A cross-coupled pair of transistors (M_5 and M_6) is added in order to prevent the conduction of current from V_{DD} to ground in the last stage. In addition, to reduce the noise injected to the bulk during switching, the biggest NFETs are implemented as triple-well devices.

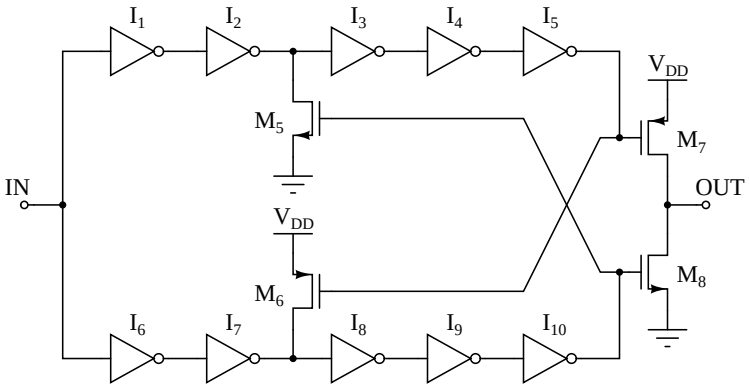

Figure 3.24: Schematic diagram of a driver used in step-down converter.

The principle of the driver operation is presented in Fig. 3.25. The clock signals are

applied to the input of the driver at time t_0. They are delayed and inverted, and appear at the gate of M_7 and M_8 at time t_1. The same signals are applied also to the gates of M_5 and M_6. The transistor M_5 conducts in the time interval from t_0 to t_1 and shorts the input of inverter I_3 to the ground. This results in small reduction of the duty cycle in the top branch. On the other hand, the transistor M_6 shorts the input of I_8 to the V_{DD} between t_2 and t_3, and thus increases the duty cycle in the bottom chain.

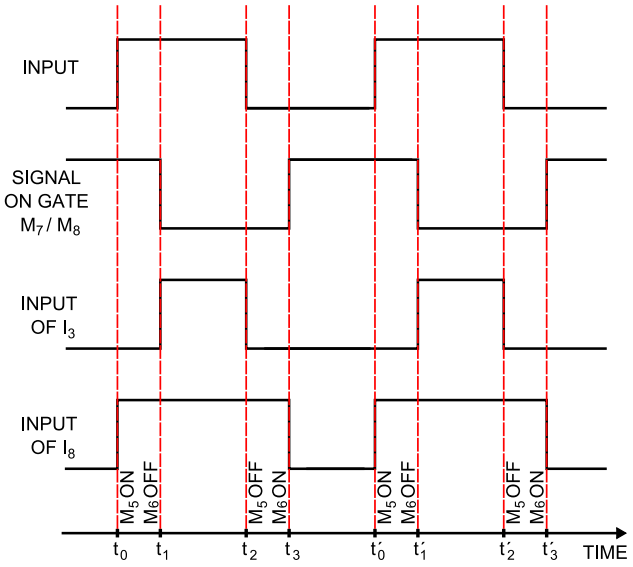

Figure 3.25: Principle of operation of a non-overlapping driver used in the design of SC DC-DC step-down converter.

Non-overlapping clock generator

Similarly to the design of the step-up converter, a non-overlapping clock generator is also an essential part of the step-down converter design and allows high power efficiency to be obtained. The architecture of the clock generator implemented in the step-down converter design is very similar to the circuit used in the previously presented charge pump. The delay line has been slightly modified compared to the schematic diagram shown in Fig. 3.8 and contains a capacitively loaded current starved inverter connected in series with the inverter circuit. The optimum dead time obtained from this circuit is 3 ns.

3.4.2 Performance of the step-down converter

All main parameters (power efficiency, output voltage and current) can be extracted on the basis of the transient analysis of the circuit. Three types of characteristics (frequency,

transfer and output) have to be investigated in order to evaluate the optimum switching frequency, input voltage range and output current range.

Simulation results of the step-down converter

Figure 3.26 shows a voltage waveform from the Cadence Virtuoso Spectre Circuit Simulator. A simulation was performed for a converter supplied with $V_{INavg} = 1.9\,\mathrm{V}$ and loaded with $15\,\Omega$ resistor. This gives a nominal output current of $I_{OUTrms} = 61.7\,\mathrm{mA}$ for the output voltage of $V_{OUTrms} = 926\,\mathrm{mV}$. The calculated input current is $I_{INavg} = 30.9\,\mathrm{mA}$ and the power efficiency is 97 %. This test was made for the switching frequency of 1 MHz, but no packaging components have been taken into account. The peak-to-peak value of the voltage ripples calculated for $C_L = 200\,\mathrm{nF}$ is around $V_{OUTp-p} = 20\,\mathrm{mV}$.

In order to reproduce the conditions corresponding to reality, additional parasitic elements must be incorporated into the simulation cell. These packaging components (inductance of 0.5 nH representing the bondwires) change the time response of the converter quite drastically. Very fast (few hundreds of MHz with rising and falling edge far below 1 ns) voltage spikes are observed at the input and the output of the circuit. The mechanism of their creation was briefly presented in Section 3.2.3. The effect itself is depicted in Fig. 3.27 and 3.28.

The peak-to-peak voltage of the spikes observed at the output is around $V_{OUTp-p} = 260\,\mathrm{mV}$. This result has been obtained from simulation in which the bond wire inductance of 0.5 nH was assumed. Due to the fact, that the spikes are symmetrical they do not affect the power efficiency at all.

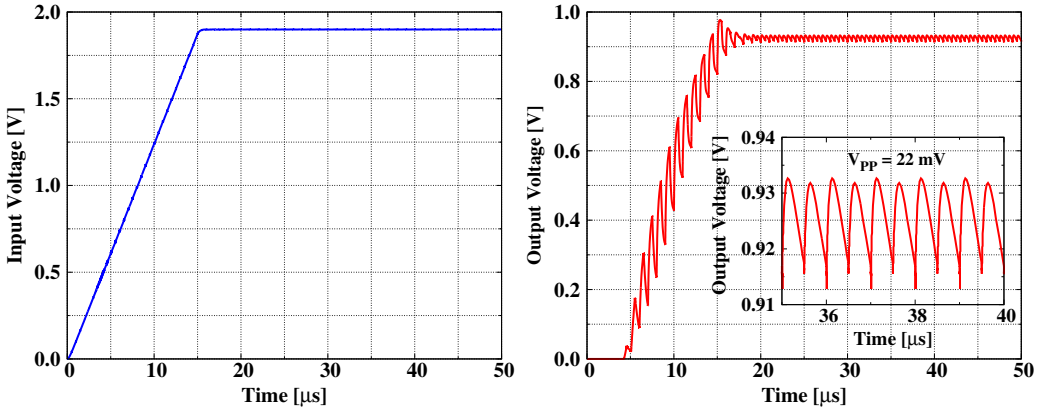

Figure 3.26: Simulated time response of the switched capacitor DC-DC step-down converter.

Figures 3.29, 3.30 and 3.31 show the three characteristics used for the circuit

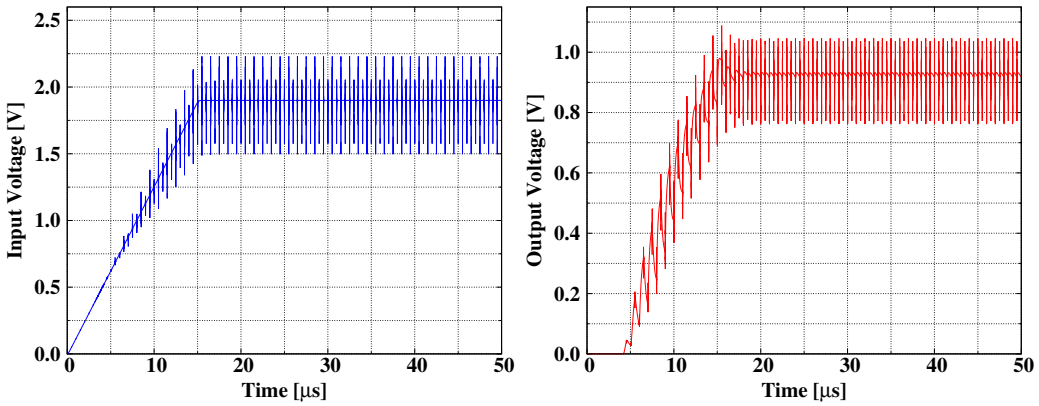

Figure 3.27: Simulated time response of the switched capacitor DC-DC step-down converter, including all package components.

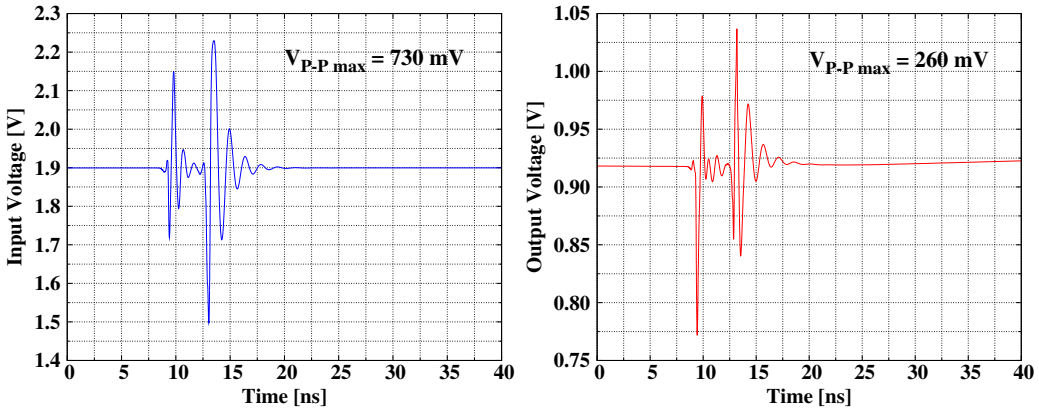

Figure 3.28: Voltage spikes observed at the input (left) and output (right) of the switched capacitor DC-DC step-down converter.

evaluation. The first of them, a frequency response (Fig. 3.29), is used to estimate the optimum value of a switching frequency, which in this case was chosen to be 1 MHz. Actually, the power efficiency does not change significantly between 500 kHz and 1 MHz. The highest possible value was chosen in order to minimise the output voltage ripples.

The transfer characteristic depicted in Fig. 3.30 shows the dependence between the supply voltage and the output voltage or the power efficiency. Although the nominal input voltage is meant to be 1.9 V, the converter can operate very efficiently over a wide input voltage range (between 1.0 V and 2.6 V). Additionally, higher supply voltage means better driving capability, hence according to the results obtained from Spectre, the step-down converter can achieve the power efficiency of 98 %.

Although the nominal output current from the step-down converter is assumed to be 60 mA nothing prevents the circuit operation with higher loads. This is confirmed

by the output characteristic shown in Fig. 3.31. For example, a twofold increase in current consumption corresponds to the power efficiency drop of just 2 %. Such a good performance of the converter is guaranteed by its very low output resistance, which is less than 0.4 Ω. Thus, it reduces conduction losses and makes the design less sensitive the load variations.

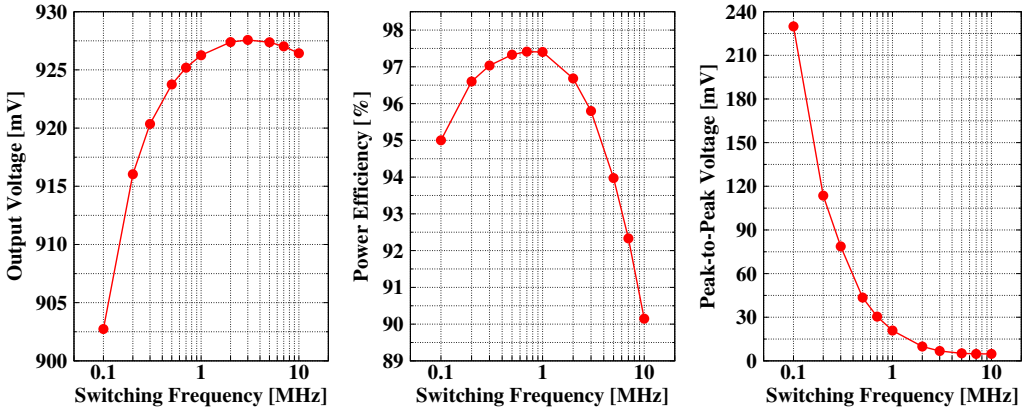

Figure 3.29: Output voltage, power efficiency and output voltage ripples versus switching frequency simulated for the SC DC-DC step-down converter.

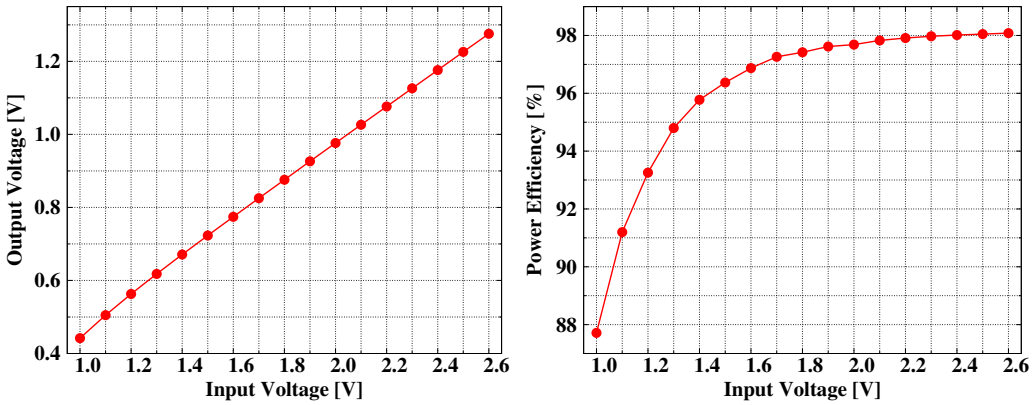

Figure 3.30: Simulated transfer characteristics of the step-down converter, the output voltage (left) and the power efficiency (right) as a function of the input voltage.

Test results of the step-down converter

The test setup and test methodology of the presented switched capacitor DC-DC step-down converter are the same as those for the step-up converter and have already been

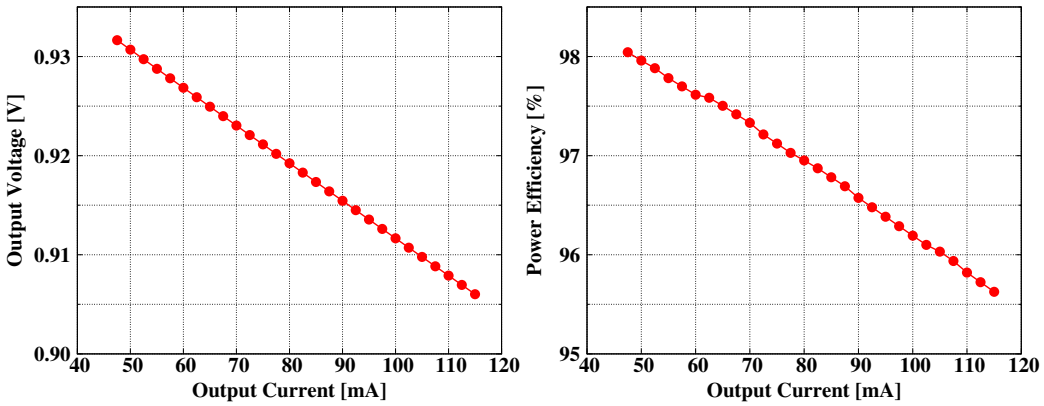

Figure 3.31: Simulated output characteristics of the step-down converter, the output voltage (left) and the power efficiency (right) as a function of the output current.

discussed in Section 3.2.3. Thus, this paragraph contains only the presentation of the measurement results. All the measurements were performed at room temperature.

The waveform in Fig. 3.32 shows the voltage signal measured with the oscilloscope at the output of the step-down converter. The measured RMS value is above $V_{OUTrms} = 0.88\,\mathrm{V}$. The circuit was supplied with $V_{INavg} = 1.9\,\mathrm{V}$ from an external DC voltage source. The input and output current were measured to be $I_{INavg} = 29.5\,\mathrm{mA}$ and $I_{OUTrms} = 58.4\,\mathrm{mA}$ respectively. The power efficiency of the step-down converter, defined as $\eta_P = (V_{OUTrms} \cdot I_{OUTrms}) / (V_{INavg} \cdot I_{INavg})$ was calculated to be higher than 91 %.

As expected from simulations, the voltage spikes appear at the output of the converter. Figure 3.33 shows a magnification of the waveform fragment containing a voltage spike. Its peak-to-peak value is higher than 200 mV and it corresponds to a total bond wire inductance of approximately 0.4 nH - 0.5 nH.

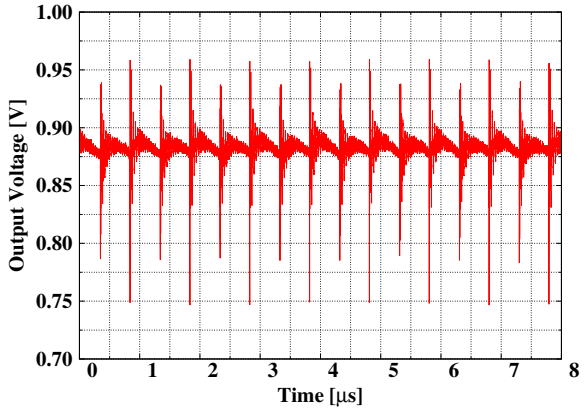

Figure 3.32: Measured transient response of the step-down converter.

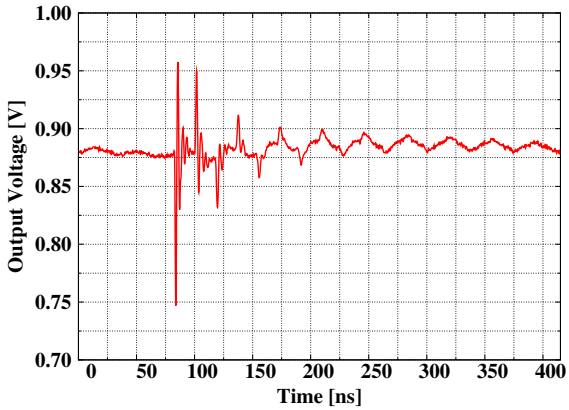

Figure 3.33: Voltage spike measured at the output of the step-down converter.

In order to fully evaluate the converter performance, three characteristics (frequency, transfer and output) have been measured. The following paragraphs present the results collected during the tests of two switched capacitor DC-DC step-down converters laid out on the same chip.

Figure 3.34 shows the frequency characteristics, measured for two step-down converters, supplied with 1.9 V and loaded with a resistor of 15 Ω. The switching frequency was swept between 100 kHz and 10 MHz. In general, the shape of the curves agrees with the simulation results, however, the output voltage and the power efficiency are systematically lower by about 5 %, compared to the simulation results shown in Fig. 3.29. For the (nominal) switching frequency of 1 MHz the measured efficiency is around 92 % instead of expected 97 %. There is also a relatively wide range of frequencies (between 500 kHz and 1 MHz), where the power efficiency is practically frequency independent. The same effect has already been observed in the step-up converter and it has the advantage that there is no need for a very precise clock.

Transfer characteristics, shown in Fig. 3.35, were measured for the input (supply) voltages between 1.0 V and 2.6 V. During the test, the step-down converter was loaded with a 15 Ω resistor and clocked with 1 MHz. The measurements confirm the expectations. The presented converter works as a divider-by-2 in a wide range of input voltages. Additionally, the power efficiency increases for higher input voltages. Thus, the performance of a converter used in the analogue power supply line, providing 1.2 V for the output current of 30 mA, will be even better.

The output characteristics are shown in Fig. 3.36. They were evaluated by applying a variable load at the output of the converters, resulting in the variation of the output current between 45 mA and 115 mA.

The measured output resistance is 1.2 Ω. and it is approximately three times higher

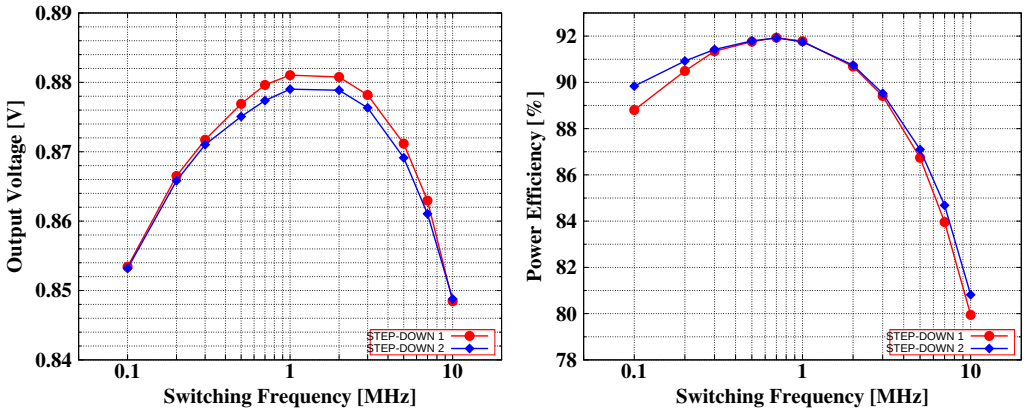

Figure 3.34: Measured values of the output voltage and the power efficiency of two step-down converters as a function of the switching frequency.

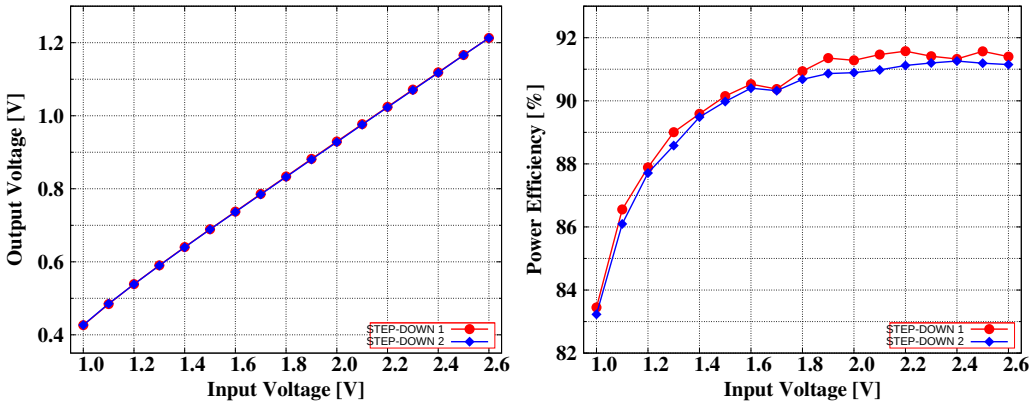

Figure 3.35: Measured transfer characteristics of two step-down converters, the output voltage (left) and the power efficiency (right) as a function of the input voltage.

in comparison to the value calculated from simulations. This unexpectedly higher output resistance seems to be the reason for the lower efficiency compared to the simulation. Assuming the output current of 60 mA, the increased resistance corresponds to power loss of around 3.1 mW, which then represents 5.5 % of the total output power. The curves representing the power efficiency in Fig. 3.36 are parallel, but the power efficiency measured for the second step-down converter is systematically lower by about 1 % in comparison with the first converter. Assuming a constant supply voltage, the only source of the observed discrepancy can the way the input current is measured. It has been calculated that a 1 % change in the power efficiency is observed when one changes the input current by around 1.2 mA. It should be noted that according to the Tektronix TCP312 specification [104] the DC measurement accuracy is ± 3 % which in this case

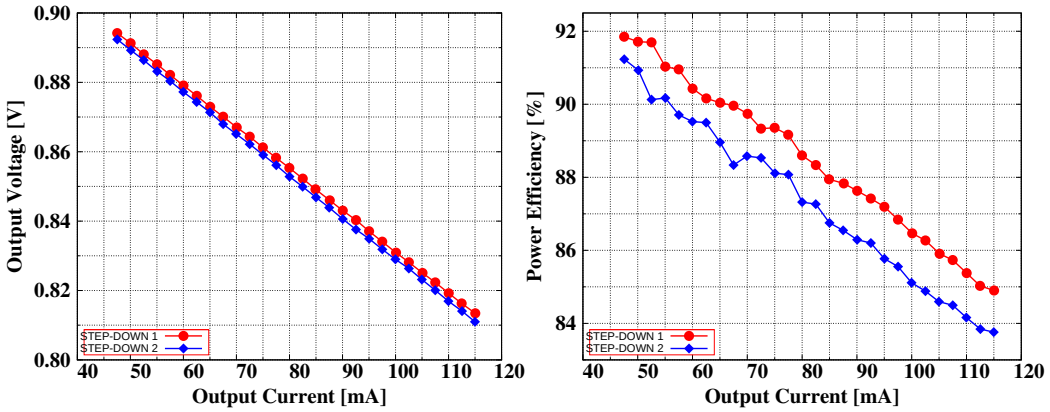

Figure 3.36: Measured output characteristics of two step-down converters, the output voltage (left) and the power efficiency (right) as a function of the output current.

corresponds to 1.8 mA.

It is also important to localise the sources of the parasitic output resistance. Among them one can enumerate: the parasitic resistance of the metal lines laid out on the chip, the resistance of the metal traces on the PCB, the resistance of the cables, etc. It was calculated that the total parasitic resistance of the metal path between the chip and the connector should not exceed 20 mΩ. The total resistance of three parallel aluminium bond wires is also in the same range. The resistance of the metal wiring (together with the vias between the metal levels), connecting the output of the converter to the pad is around 110 mΩ. One must not forget about the spread resistance related to the metal grid which tightly covers each MOS switch and guarantees a uniform current flow.

Post-radiation test results of the step-down converter

The irradiation tests of the step-down converter were performed using the same X-ray facility as described in Section 2.3. During the test the step-down converter was irradiated in steps up to a TID of 200 Mrad in 80 hours at room temperature. Then the PCB with the biased chip was kept in an oven for annealing for 168 hours at 100 °C.

Plots shown in Fig. 3.37 present the evolution of the output voltage and the power efficiency measured after several irradiation steps. It is worth mentioning that all transistors used in the presented design of a step-down converter are thick gate oxide devices. Thus, it is expected to be more sensitive to radiation induced effects, threshold voltage shift and leakage current.

However, the post-irradiation performance of the converter seems to be satisfactory. The measured relative output voltage drop is less than 1.2 %. The power efficiency after

irradiation up to 200 Mrad varies by less than 5 % and still remains above 87 %. Annealing at high temperature partially restores the converter performance and the power efficiency rises back, up to 90 %.

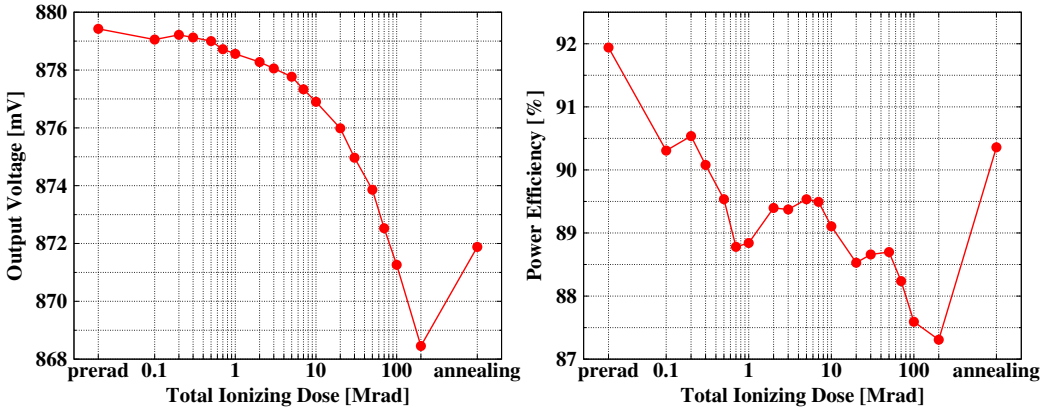

Figure 3.37: Measured value of the output voltage (left) and the power efficiency (right) for different TIDs.

A degradation of the converter output characteristics (Fig. 3.38) is visible. The output resistance after the irradiation was measured to be around 1.36 Ω and results in the efficiency drop due to higher conduction losses. Annealing at high temperature decreases the output resistance to 1.30 Ω.

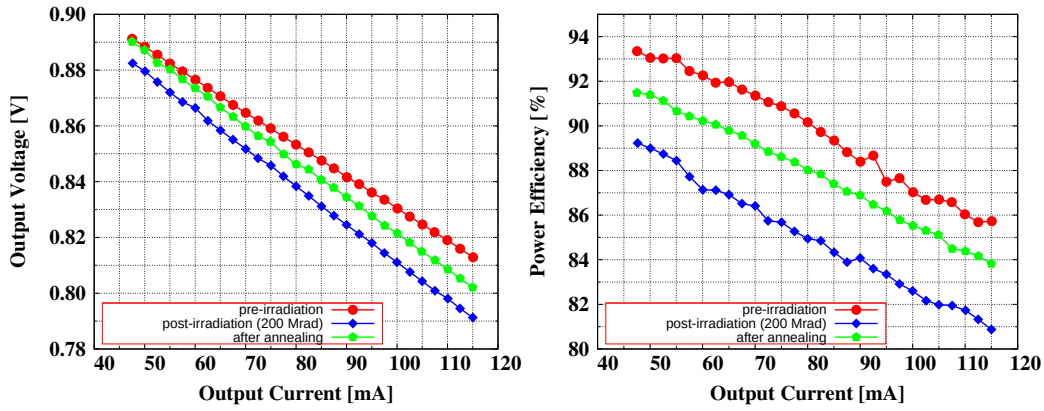

Figure 3.38: Measured output characteristics of the SC DC-DC step-down converter before irradiation (red line), after irradiation (blue line) and after annealing (green line).

3.5 Design of the DCDC013 chip

The DCDC013 chip contains the switched capacitor DC-DC converters previously detailed. Each ASIC contains four power converters, two step-up and two step-down. It has been designed and manufactured using an IBM CMOS process with the 130 nm lithography node and including eight metal levels. The layout and the microphotograph of the entire DCDC013 chip is shown in Fig. 3.39. The size of a die is $2 \times 2\,\mathrm{mm}^2$. The layouts of each circuit are described separately in the following Sections 3.5.1 and 3.5.2 for the step-up and step-down, respectively.

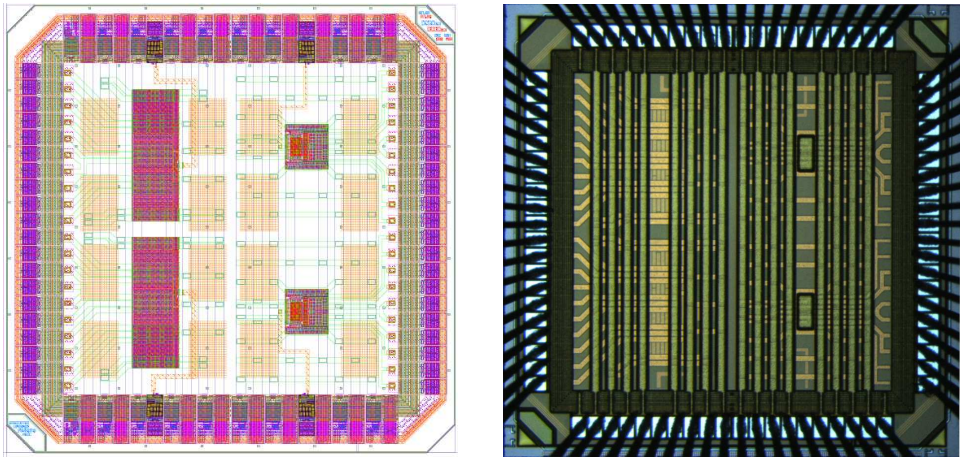

Figure 3.39: Layout of the DCDC013 from Cadence Virtuoso Layout Suite (left) and the microphotograph of the chip bonded to a PCB (right).

Each chip contains 80 pads (20 power pads, 20 ground pads and 40 signal pads, including 4 digital interfaces to provide clock signals to converters). Simulations showed that the parasitic inductance of the bondwires results in voltage spikes observed at the input and output of the circuitry. Hence, in order to minimise this effect power pads / wires and ground pads / wires are interleaved. This technique allows the reduction of the effective inductance roughly by a factor equal to the number of the pad pairs (power and ground) [105]. One should note that on the other hand the effective capacitance of bonding increases due to the coupling between wires.

In order to minimise the resistive losses between the chip and the external components, multiple pads have been used. Additionally, the SMD capacitors are soldered on a PCB very close to the chip.

3.5.1 Layout of switched capacitor DC-DC step-up converter

The prototype of the charge pump is 190 µm wide and 200 µm high. Thus, the total area of silicon is less than 0.04 mm^2. The layout of the device is shown in Fig. 3.40.

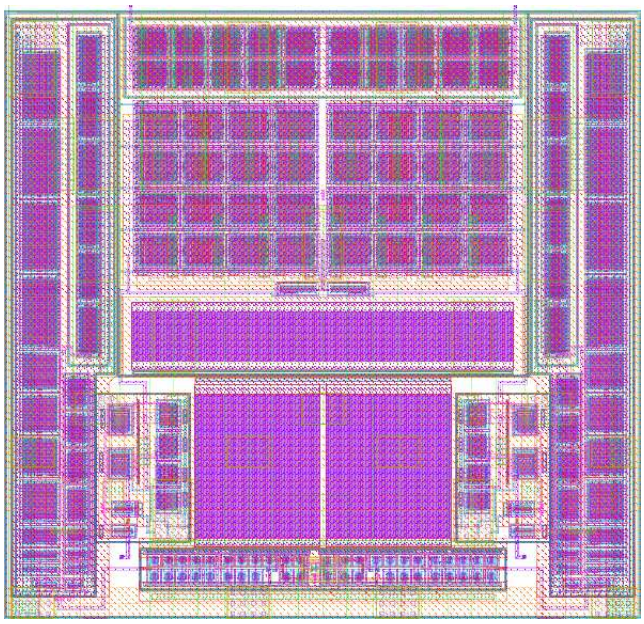

Figure 3.40: Layout of the switched capacitor DC-DC step-up converter.

The power switches of both types and the auxiliary charge pump, together with the integrated capacitance C_A, occupy approximately 35 % of the total silicon area. The two scaled inverter chains used as MOSFET drivers occupy approximately 31 %. The non-overlapping clock generator, containing two integrated capacitances of 1 pF each, with the level shifter circuits takes 24 % of silicon area. The remaining 10 % is used for the substrate contacts, guard-rings and fillings in order to satisfy the DRC rules.

As it is assumed presently, the intrinsic radiation hardness of the technology will be sufficient, hence no dedicated radiation tolerant layout techniques have been used in the design.

3.5.2 Layout of switched capacitor DC-DC step-down converter

The layout of a switched capacitor DC-DC step-down converter is shown in Fig. 3.41. The converter is 210 µm wide and 590 µm high, so it occupies slightly more than 0.12 mm^2 of silicon area. Two identical prototype step-down converters are implemented on each prototype ASIC.

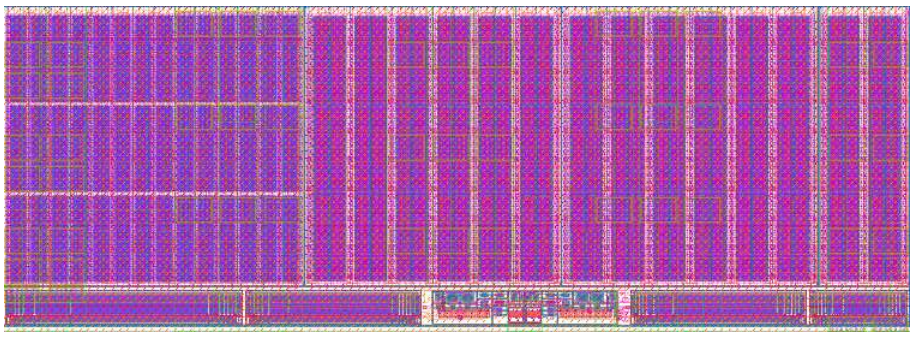

Figure 3.41: Layout of the switched capacitor DC-DC step-down converter.

Almost 80 % of the silicon area is occupied by the MOSFET switches M_1 through M_4 from the core of the converter shown in Fig. 3.23. The remaining 20 % of space is used by: drivers (9 %), non-overlapping clock generator (3 %), substrate connection and guardrings (8 %).

Similarly to the previous case of the step-up converter, the SC DC-DC step down converter was laid out using no dedicated radiation tolerant techniques (e.g. enclosed-geometry transistors). However, all necessary precautions were taken to minimise the leakage current and prevent the circuit from latching up.

3.6 Conclusions on the DCDC013 development

DCDC013 chip, presented in this chapter contains two prototype designs of switched capacitor DC-DC converters. The chip was designed in IBM 130 nm CMOS technology. Currently, these devices are considered to be key elements of the proposed powering schemes in the upgraded silicon tracker for the ATLAS experiment.

Both devices are characterised with very high power efficiency 85 % and 91 %, respectively for the step-up and step-down converter. Other remaining parameters, including the output voltage for a given load, are compatible with the specification. The results from the measurements agree quite well with simulations. It is worth noting that the presented SC DC-DC step-down converter has already been used as an alternative powering block in a CMS Binary Chip (CBC) [106] designed at Imperial College London and RAL in United Kingdom, and has been shown to operate well on this front-end chip.

There are two main issues discovered during the development of the prototypes. The first of them is related to the poor quality of output voltage from the converters caused by the parasitic inductance of the bond wires. Currently, there are several possible solution considered. One of them assumes replacing bond wires with bump bonding in order to

discard elements introducing parasitic inductance to the circuit. Another idea assumes using capacitors which can be bump bonded directly on the surface of the silicon die.

The irradiation tests of the DCDC013 chip show a decrease in the converter performance. This effect starts to be clearly visible above the TID of few tens of Mrad and is caused by the use of irradiation sensitive, thick gate oxide transistors. This aspect of the design should be thoroughly investigated and fixed in the final design, thus employing the Enclosed Layout Transistors (ELTs) is highly recommended.

The observed post-irradiation decrease in the power efficiency of the presented converters is mainly caused by the increase of conduction losses occurring in the power switches. The radiation induced threshold voltage shift effect makes the on-current in the *p*-channel transistors decrease and one should note that the thick gate oxide PFETs are present in both converter designs, step-up and step-down. The solution to this problem would be to increase the size of the switches in order to guarantee the low on-resistance also after the irradiation. It is however worth noting that bigger switches have higher gate capacitance and will result in potential increase of the switching loss. Hence, the power budget analysis for each converter should be investigated once more.

The increase of the conduction loss is not the only source of the converter inefficiency after irradiation. The inverters used in the power MOSFET switches are well balanced assuming the pre-irradiation values of the threshold voltage. The drivers' performance however decrease with the TID due to V_{th} shift. The radiation makes the NMOS transistors easier and PMOS transistors more difficult to switch on. This leads to an increase in the cross conduction current, which in the case of the large inverters may have a significant contribution to the overall power budget of the converter. Hence, analysing the data from Chapter 2, one may consider intentionally unbalancing the inverters to obtain the best performance in a moderate dose range.

Chapter 4

Linear voltage regulators for the serial powering scheme

A linear voltage regulator is an electronic circuit which uses a voltage controlled current source in order to provide a constant, predetermined output voltage, regardless of changes of the load current or the input voltage. All linear voltage regulators are step-down devices. This means that the output voltage is always lower than the input voltage.

In commercial applications, linear voltage regulators are commonly used together with the DC-DC converters. Very often a linear regulator follows a step-down DC-DC buck converter. This solution allows the designer to minimise the voltage drop across the pass element and in consequence to minimise the overall power losses in a regulator.

It has already been shown in Chapter 1 (Fig. 1.10) that a cascade of a DC-DC converter and a linear regulator is also foreseen for the future Inner Detector electronics upgrade, but in this particular case a switched capacitor DC-DC step-up converter will be used. Together, they will be used to provide high quality supply voltage of 1.2 V (obtained from 0.9 V), required for the analogue front-end.

4.1 Basics of the linear voltage regulators

The generic architecture of a linear voltage regulator is shown in Fig. 4.1. The diagram consists of five blocks, namely series pass element (transistor), error amplifier, sampling network (resistive divider), source of stable reference voltage and load. The overall operation principle of a linear voltage regulator is simple. The output voltage (V_{OUT}) is constantly sensed by the control circuit, implemented as a resistive divider. The output voltage is controlled using a feedback loop, which in some cases requires compensation to

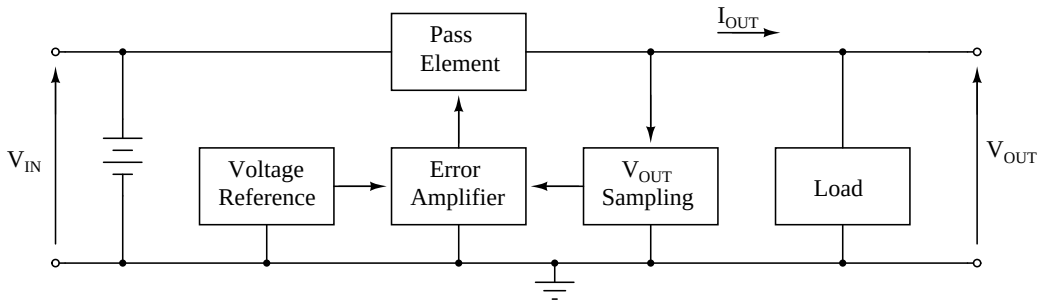

Figure 4.1: Block diagram representing an architecture of a linear voltage regulator.

maintain the system stability. Any voltage regulator also needs a stable reference voltage source [76]. The error amplifier senses the voltage difference between its inputs and feeds it back to the gate of the pass transistor, changing its overdrive voltage. The pass element is used as a voltage-controlled current source. Thus, while the gate voltage is changed the drain current is tuned, so the output voltage remains constant.

4.2 Characterisation of linear voltage regulators

According to [107], there are three main aspects of the linear voltage regulator design: regulating performance, current efficiency and operating voltage. These aspects are fully described by a set of following parameters [108]:

- Dropout voltage, denoted by V_{DO}, defines a minimum differential voltage between the input and the output pin at which the regulator is still able to operate properly. The dropout voltage is in fact the saturation voltage (V_{DSsat}) of the pass transistor. Thus, its minimum allowable value is limited to 80 mV – 130 mV, corresponding to $3U_T - 5U_T$[1] [109]. To obtain a minimum voltage drop across the pass device for the maximum current it must have a large W/L ratio.

- Line regulation (input regulation) determines the output voltage change (ΔV_{OUT}) triggered by a certain voltage change (ΔV_{IN}) at the input of the regulator, measured for a given value of the output current.

$$\text{Line regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \cdot 100\,\% \tag{4.1}$$

[1]Thermal voltage is defined as $U_T = kT/q$, where k is the Boltzmann constant, q is the electron's charge and T is temperature. The value of thermal voltage at room temperature is approximately 26 mV.

- Load regulation measures the capability of the regulator to maintain a constant, specified output voltage despite the changes of the load current (ΔI_{OUT}).

$$\text{Load regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \cdot 100\,\% \tag{4.2}$$

- Temperature dependence parameter describes the temperature stability of the regulator. The temperature sensitivity of the regulator comes mainly from two sources, the temperature coefficient of the bandgap voltage reference [76] circuit[2] and the temperature drift of the input offset voltage.

$$\text{Temperature dependence parameter} = \frac{\Delta V_{OUT}}{\Delta T} \tag{4.3}$$

- Transient response (transient output voltage variation) measures the maximum allowable output voltage change caused by a transient load current step. Transient response (ΔV_{TRmax}) is a function of four parameters: system time response (Δt), maximum load current (I_{OUTmax}), output capacitance (C_{OUT}) and its Equivalent Series Resistance, and it is defined as follows:

$$\Delta V_{TRmax} = \frac{I_{OUTmax}}{C_{OUT} + C_b}\Delta t + \Delta V_{ESR}. \tag{4.4}$$

  Voltage variation due to the parasitic ESR of the output capacitor is denoted as ΔV_{ESR}. Additionally, a bypass capacitor C_b can be connected in parallel to the load in order to improve the transient response of the circuit, hence it has also been included in the Eq. 4.4.

- Quiescent current (I_Q) can be expressed as the difference between the input (I_{IN}) and the output (I_{OUT}) current.

$$I_Q = I_{IN} - I_{OUT} \tag{4.5}$$

  The quiescent current is practically independent of the load conditions and consists of the bandgap voltage reference circuit bias current, the currents flowing in the error amplifier and in the sampling circuit.

- Power Supply Rejection Ratio (PSRR) measures the ability of the regulator to suppress output voltage fluctuations (V_{OUTp-p}) caused by the change in the input

[2]The temperature coefficient is defined as $\partial V_{REF}/\partial T$.

voltage supply (V_{INp-p}). It can also be identified as an AC voltage gain from the input node of the regulator to the output node, measured in dB over a spectrum of frequencies.

$$PSRR = \left(\frac{V_{OUTp-p}}{V_{INp-p}} \right)_{f \in [0,\infty)} \tag{4.6}$$

- Output noise voltage is the RMS value of the output noise voltage, measured over a certain frequency spectrum, under the conditions of a constant load current and clean input voltage.

4.3 Power considerations

In order to maintain a very high power efficiency for the serial powering scheme, it is very important to keep the power efficiency of each building block at the highest possible level.

The power efficiency of a linear voltage regulator is defined as the ratio of the output power (P_{OUT}) to the input power (P_{IN}), delivered to the circuit from the voltage supply. By applying Joule's law, one can get the following expression for the power efficiency:

$$\eta_P = \frac{P_{OUT}}{P_{IN}} = \frac{I_{OUT} \cdot V_{OUT}}{(I_{IN} + I_Q) V_{IN}}. \tag{4.7}$$

The above formula shows that the power efficiency of the voltage regulator will never reach 100 %. This is due to a non-zero quiescent current (I_Q) of the regulator and the non-zero dropout voltage. Thus, it is important to make the drouput voltage as low as possible.

The operating conditions for the voltage regulator, planned to be used in the serial powering scheme, are very well defined. The regulator is meant to maintain a constant voltage of 1.2 V at its output. The input voltage could vary between approximately 1.3 V and 1.6 V, depending on the load conditions. For the nominal current of 30 mA, the input voltage is as high as 1.55 V. This corresponds to a voltage drop of 350 mV across the pass element. However under heavy load conditions the input voltage can drop down to 1.3 V. Thus, the dropout voltage of the regulator should be at the level of 100 mV or less.

4.4 Main topologies of linear voltage regulators

There are only two main linear voltage architectures. A conventional (classical) voltage regulator uses an *n*-channel transistor in a source follower configuration, while a low-dropout (LDO) voltage regulator employs a *p*-channel device in a common source architecture. A brief comparison of both topologies is presented below.

In many commercial applications voltage regulators using bipolar transistors as pass devices are still very common, mainly because they can provide high output currents. The technology planned to be used for the upgrade of the front-end electronics does not support bipolar devices, so the regulators described in this chapter employ MOSFETs.

4.4.1 Linear voltage regulator based on *n*-channel transistor

A schematic diagram of a conventional linear voltage regulator is shown in Fig. 4.2. The output voltage is sensed via the resistive voltage divider (R_{F1} and R_{F2}) and compared with the reference voltage. Then the error signal is fed back to the gate of the NFET, M_{PASS}.

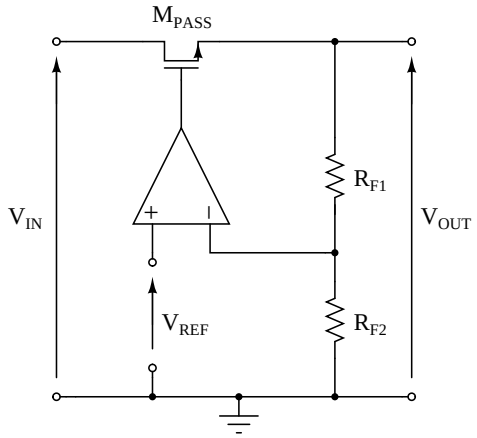

Figure 4.2: Schematic diagram of a simple, classical linear voltage regulator employing an *n*-channel pass transistor.

The regulator using an *n*-channel transistor has a big advantage over the architecture employing a *p*-channel transistor, because it is inherently stable due to a very low output impedance of the source follower stage [110]. Additionally, the higher carrier mobility results in lower on-resistance of the NFET in comparison with the identical PFET and the voltage drop across the pass device, for a certain current, will always be lower [111].

On the other hand, a conventional regulator requires a positive drive signal with respect to the output. It implicates higher dropout voltage, unless some auxiliary circuitry (i.e. a charge pump) is introduced into the design. Such an issue can be solved by

employing a zero-V_{th} NFET[3], a transistor with nearly zero threshold voltage. This allows a sufficiently high overdrive voltage to be reached, and such a regulator becomes in fact an LDO regulator.

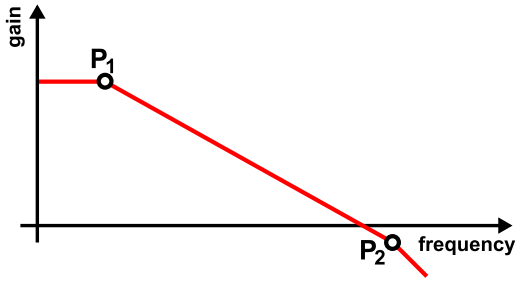

Figure 4.3: Frequency response of a clasical NFET-based linear voltage regulator.

Figure 4.3 shows the frequency response of an NFET-based linear voltage regulator. A conventional voltage regulator has two poles, denoted as P_1 and P_2. The dominant, low frequency pole P_1 comes from the error amplifier. The pole P_2 is a product of the low output impedance of the source follower and the output capacitor. Usually, P_2 is near or greater than the unity-gain bandwidth so a good phase margin is relatively easy to obtain. One should note that in order to provide good filtering capability of fast AC signals, adding a large output capacitance can be recommended, but it is not required from the standpoint of stability.

4.4.2 Low-dropout linear voltage regulator based on *p*-channel transistor

Figure 4.4 shows a schematic diagram of a linear voltage regulator employing a *p*-channel transistor as a pass element. The orientation of the pass element significantly changes the characteristics of the regulator. The pass transistor is used in a common-source topology and becomes an amplifying stage. This produces additional $-90°$ phase shift and makes the voltage regulator based on a PFET inherently unstable.

To achieve control loop stability, the PFET-based voltage regulator requires an external output capacitor with a non-zero Equivalent Series Resistance. ESR compensation is commonly used, mainly due to its simplicity. A large output capacitor also guarantees better filtering capability for high frequencies. In some specific cases it is required to

[3]Zero-V_{th} NFET also called "natural" transistor is an optional device available in some modern CMOS technologies, obtained by blocking the *p*-well implants during the manufacturing process.

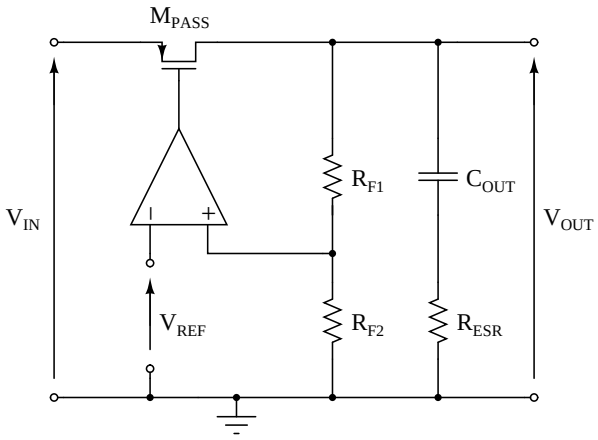

Figure 4.4: Schematic diagram of a simple LDO linear voltage regulator employing a *p*-channel pass transistor.

obtain a stable system without the use of any external components. This can be achieved, but usually one has to pay a price in the system complexity. Two interesting solutions to this problem can be found in [112] and [113].

The frequency response of an LDO regulator employing a *p*-channel transistor, shown in Fig. 4.5, is more complex that the frequency response of a regulator, based on *n*-channel device in a source-follower configuration.

A non compensated LDO voltage regulator has two low frequency poles, P_1 and P_2. A dominant pole P_1 is a product of the output capacitance and the high impedance seen from the output of the regulator. The second pole, P_2, is an internal pole of the error amplifier. The frequency response of such a non compensated voltage regulator is show in Fig. 4.5a.

The regulator becomes stable if a capacitor with a parasitic ESR is added at the output. By doing this the designer introduces another pole (P_3) and a Right Half-Plane (RHP) zero (Z_0) into the circuit. Zero Z_0 is absolutely essential for the control loop stability, because it produces a $+90^\circ$ phase shift, and thus it makes the linear regulator stable. The third pole (P_3) is usually not an issue, unless it is located in a high frequency region, above the unity-gain bandwidth. The frequency response of an LDO compensated with an external capacitor is shown in Fig. 4.5b.

One should note that for a given value of output current and output capacitor, there is a minimum and maximum value of the ESR, for which the regulator remains stable. This range is called the "tunnel of death" [108]. The pole-zero compensation technique is successful if the zero is equal or close to the pole. Keeping the ESR inside the narrow "tunnel of death" is not a trivial task, since the resistance can vary by orders of magnitude

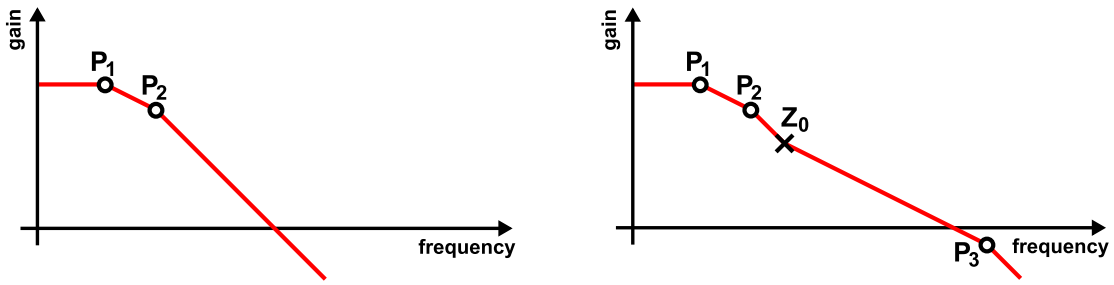

Figure 4.5: Frequency response of a PFET-based LDO voltage regulator without (left) and with (right) the compensation.

(between few tens of mΩ and few Ω), depending on the type of capacitor, the temperature and the frequency. For example, if the ESR decreases, the zero Z_0 starts moving towards high frequencies and finally exceeds the unity-gain bandwidth, the system would become unstable. On the other hand, if the ESR increases, the pole P_3 moves towards lower frequencies, again resulting in system instability.

4.5 Design of the low-dropout regulator using a *n*-channel MOS device for voltage regulation

The first of two linear voltage regulators prototypes presented in this thesis is based on an *n*-channel pass transistor. The IBM 130 nm CMOS process offers the zero-V_{th} NMOS transistors, hence then can be used in the design.

The expected output voltage from the switched capacitor DC-DC step-up converter is around 1.55 V, assuming the nominal load conditions ($I_{OUT} = 30$ mA). This voltage may however vary, depending on the current consumption in the analogue front-end electronics[4]. The minimal output voltage from the step-up converter, for a heavy load, is expected to be approximately 1.3 V.

Figure 4.6 shows a schematic diagram of the prototype linear voltage regulator based on a zero-V_{th} NFET. The design consists of the following blocks: bandgap voltage reference circuitry with the *RC* filter, error amplifier, pass transistor (M_{PASS}), resistive sensing network (R_{F1}, R_{F2}), compensation network (C_{C1}, C_{C2}) and load. The load is realised with an external capacitor C_{OUT} (with R_{ESR}) and a resistor R_L.

The voltage reference circuit provides a constant voltage of 637 mV. It was designed

[4]The current consumption in the analogue front-end electronics of the ABCN-13 chips is expected to be rather constant (around 30 mA in case of 128 and around 70 mA in case of 256 read-out channels for the short silicon strip sensors). However, some fluctuations (not larger than ±20 % of the nominal current) are unavoidable.

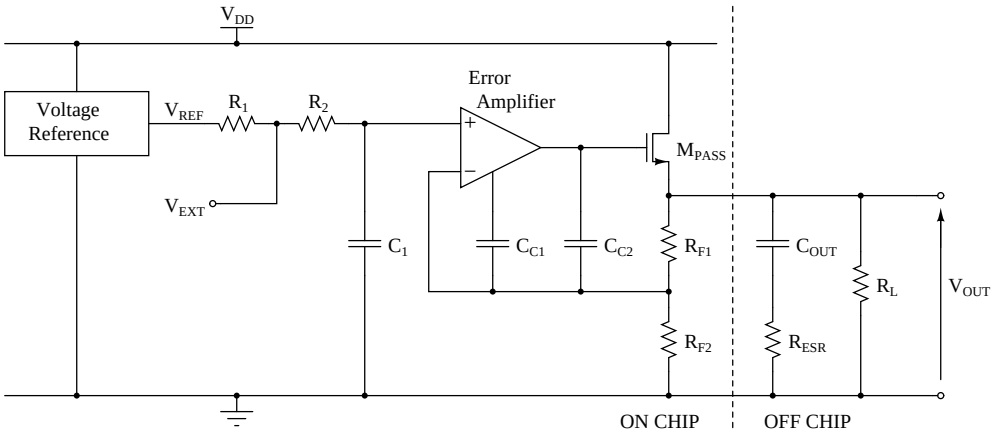

Figure 4.6: Schematic diagram of the linear voltage regulator prototype based on a zero-V_{th} n-channel pass transistor.

at CERN and primarily used in the GigaBit Transceiver (GBT) project. In order to assure good reference voltage quality, the output from the bandgap circuit is additionally filtered with the *R*-*C* network consisting of two identical resistors ($R_1 = R_2 = 50\,\mathrm{k\Omega}$) and the capacitor $C_1 = 1\,\mathrm{pF}$, fully integrated on the silicon die.

The design of the error amplifier is more complex and it will be described in detail in the next section.

The compensation network is necessary to obtain the stability of the presented voltage regulator. An extensive description of the technique called pole splitting, applied in the design, can be found in [76] and [114]. The values of the capacitors ($C_{C1} = 2.0\,\mathrm{pF}$ and $C_{C2} = 1.2\,\mathrm{pF}$) have been chosen on the basis of simulations carried out in the SPICE environment. Both capacitors are fully integrated into the chip.

The sensing network is realised with two polysilicon resistors R_{F1} and R_{F2}. The ratio of these two resistors defines the output voltage accordingly to the following formula:

$$V_{OUT} = V_{REF}\left(1 + \frac{R_{F1}}{R_{F2}}\right), \tag{4.8}$$

where V_{OUT} is the output voltage and V_{REF} is the stable reference voltage provided by the bandgap circuitry. Assuming an output voltage of 1.2 V, the ratio R_{F1}/R_{F2} must be equal to 0.884. The resistor values have been arbitrary chosen to be $R_{F1} = 50\,\mathrm{k\Omega}$ and $R_{F2} = 56\,\mathrm{k\Omega}$. This choice guarantees the output voltage a few tens of mV higher than expected 1.2 V, so the V_{OUT} is kept at correct level for all the process corners.

The load of the converter comprises the large capacitor $C_L = 100\,\mathrm{nF}$ and the load resistance, R_L. This capacitor is too big to be implemented on the chip. It must be external.

It is however possible to use a small SMD package, e.g. 0603 or smaller. For simulation reasons, the R_{ESR} of 10 mΩ is added. The exact value of R_{ESR} is not well defined and has to be measured separately for each capacitor. The load resistor is used to enforce a proper load current.

4.5.1 Design of the error amplifier

The proposed error amplifier consists of three main blocks, the current reference circuit, the first and the second amplifying stages. They are briefly described below. A schematic of the entire amplifier, used in the NFET-based voltage regulator, together with the transistors sizing can be found in Fig. 4.11 and Table 4.1, at the end of the section.

Current reference circuit

The biasing cell is realised using a threshold-referenced topology with a simple startup circuit. The circuit generates a constant current, independent of the voltage supply. This technique is known as a V_{th}-referenced source or a bootstrap reference [76]. Figure 4.7 shows a current reference circuit.

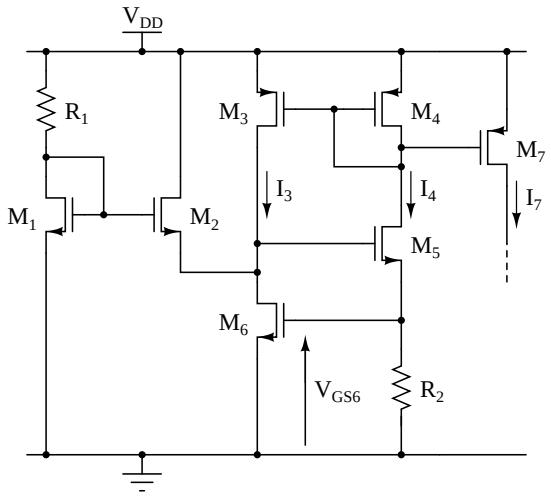

Figure 4.7: Schematic diagram of the biasing cell with the start-up circuit used in the design of the error amplifier.

The operation principle of this circuit is simple. The current mirror M_3 and M_4 ensures that currents I_3 and I_4 are equal. The current I_3, flowing through the transistor M_6, creates a gate-to-source voltage V_{GS6}. Current I_4 flowing in the second branch (through the resistor R_2) results in a voltage drop of I_4R_2, equal to V_{GS6}. By comparing these two

conditions one gets the second order equation:

$$IR_2 = V_{th} + \left(\frac{2IL_6}{\mu_{0n}C_{ox}W_6}\right)^{1/2}, \tag{4.9}$$

where $I = I_3 = I_4$ represents the unknown current, $\mu_{0n}C_{ox}$ is a technology constant, W_6 and L_6 are the width and the length of the transistor M_6, respectively. This polynomial equation has two roots, one for $I \approx 0$ and the second for a certain equilibrium voltage. In order to assure that the correct equilibrium point is chosen, the presence of some start-up circuitry is required.

The start-up circuit consists of three elements, the transistors M_1 and M_2 and the resistor R_1. The current pumped by the transistor M_2 into the drain of M_6 moves the circuit to the desired equilibrium point. After the current in M_6 increases, the voltage at the source of M_2 also rises up and the transistor shuts off.

First stage of the error amplifier

The first amplifying stage is implemented using a folded-cascode topology [76] with the NFET input pair. The simplest possible implementation of this circuit is shown in Fig. 4.8a. The folded-cascode architecture provides good input common-mode range, power-supply rejection and relatively good small signal voltage gain, which assuming ideal current sources I_1 and I_2, can be expressed in a following way:

$$A_v \approx -\frac{g_{m1} \cdot g_{m2}}{g_{ds1} \cdot g_{ds2}}, \tag{4.10}$$

where $g_{m1,2}$ and $g_{ds1,2}$ are the small signal transconductances and the drain-to-source conductances of transistors M_1 and M_2, respectively.

One should note that in some specific cases the voltage gain obtained from the folded-cascode circuit may be insufficient. There is a simple way that allows a significant boost of the voltage gain without loosing the amplifier's bandwidth. This technique is called gain-boosting. The general concept of gain-boosting is presented in Fig. 4.8b. An amplifier with a voltage gain of $-k_v$, driving the gate of transistor M_2 introduces a negative feedback loop. This leads to an increase of the output impedance of the main cascode amplifier, and hence to the increase of the voltage gain. The amplifier can be implemented as a single transistor in a common-source configuration. The modified architecture is shown in Fig. 4.8c [115]. The transistor M_3 is connected between the source and the gate of transistor M_2. The voltage gain obtained thanks to this improvement can be approximated

with the following expression:

$$A_v \approx -\frac{g_{m1} \cdot g_{m2} \cdot g_{m3}}{2g_{ds1} \cdot g_{ds2} \cdot g_{ds3}}. \tag{4.11}$$

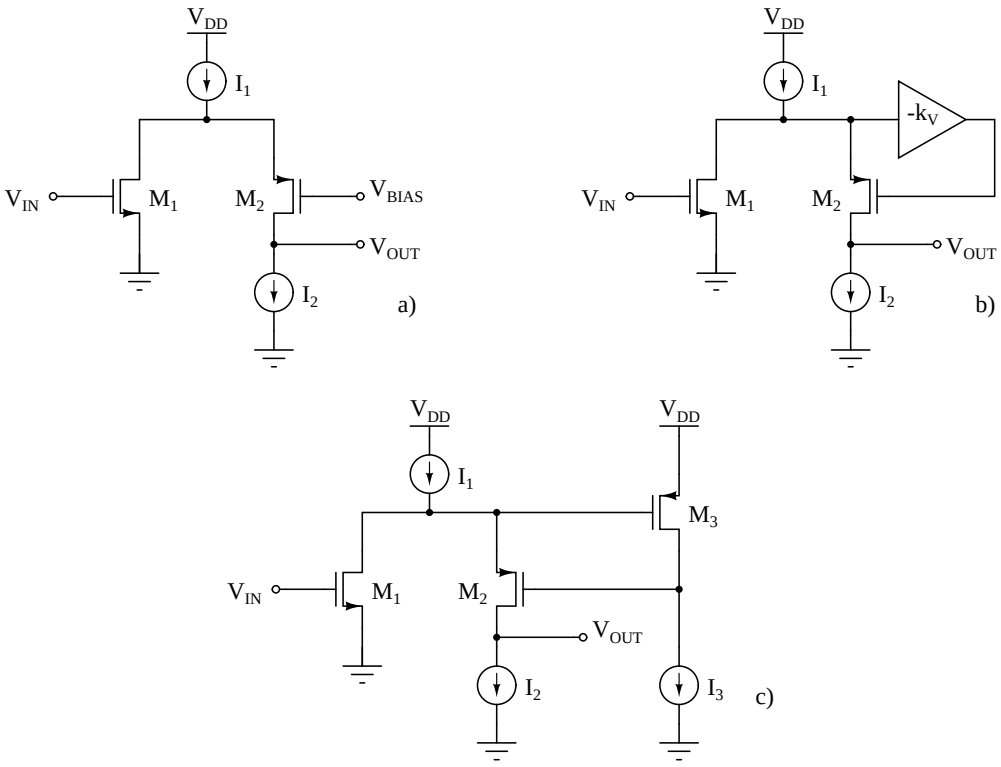

Figure 4.8: Topology of a simple folded-cascode amplifier (a), possible gain enhancement of the folded-cascode amplifier using a gain-boosting technique (b) and its practical implementation (c).

The schematic diagram of the full gain-boosted folded-cascode op amp circuitry applied in the discussed error amplifier design is shown in Fig. 4.9. The *n*-channel transistors M_{13} and M_{14} are used as the input pair. Transistors M_{21} and M_{22} are the cascoding transistors. The cascode current source realised by four NMOS transistors M_{23} through M_{26}, allows both high output impedance and high voltage gain to be obtained. Transistors M_{19} and M_{20}, connected in common source configuration act as auxiliary amplifiers (with the voltage gain of $-k_v$) from Fig. 4.8b. The transistor M_{20} helps to isolate the source of M_{22} from the output signal. Also the drain of the input transistor, M_{14}, is better isolated so the signal from the output influences the drain current to a lesser degree and thus the DC voltage gain of the amplifier increases.

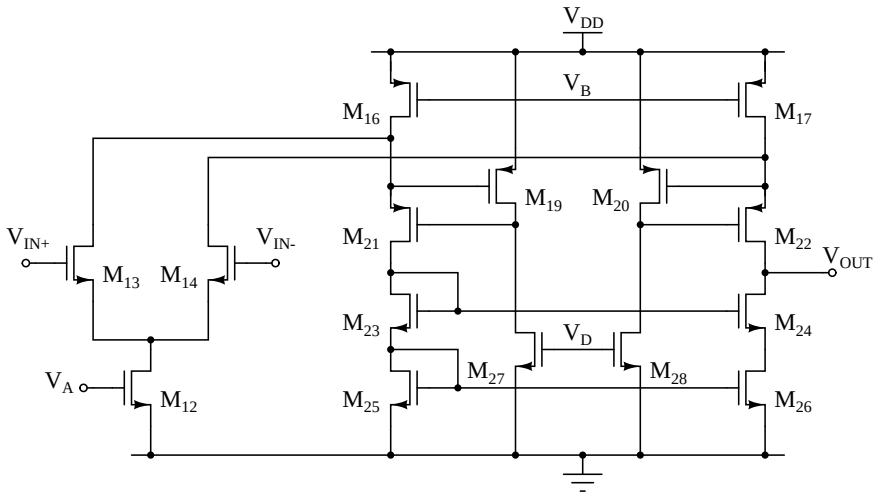

Figure 4.9: Schematic diagram of the first amplifying stage using a cascode current sink.

Second stage of the error amplifier

Due to the use of the gain-boosted folded-cascode topology, the voltage gain obtained in the first stage of the amplifier is sufficient and the second amplifying stage is not actually required to further increase the gain. One should however note that the error amplifier must drive the gate of a large pass transistor. In addition, the potential on this gate is almost as high as the supply voltage. Therefore, the second stage is necessary to operate as a level shifter driving the large gate capacitance of the pass device. Without this buffering stage the proper biasing of the transistors in the folded-cascode circuitry would not be possible.

The error amplifier used in the presented design employs a classical source follower topology [116], based on a *p*-channel transistor as the second amplifying stage. A schematic diagram of the second stage is shown in Fig. 4.10.

Although the voltage gain of the source follower is close to unity, it has the advantage of a very low output resistance. Due to that fact, the output pole of the second stage is located in the high frequency region, well beyond the unity-gain frequency. The output resistance of the presented the circuit can be approximated as:

$$R_{OUT} \approx \frac{1}{g_{m32} + g_{mb32}}. \tag{4.12}$$

where g_{m32} and g_{mb32} are the small-signal transconductance and the body transconductance of the transistor M_{32}, respectively.

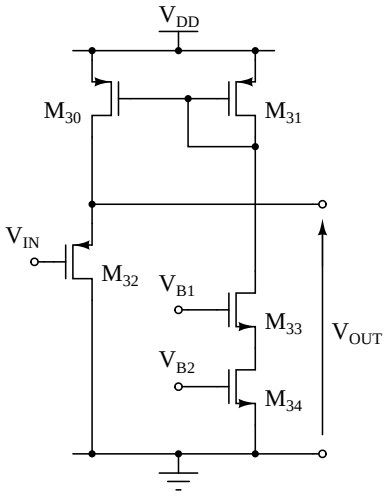

Figure 4.10: Schematic diagram of the source follower used in the design of the error amplifier.

Assuming high values of r_{ds30} and r_{ds32}[5], the small-signal voltage gain of a circuit shown in Fig. 4.10 is given by a formula:

$$A_v \approx \frac{g_{m32} \cdot r_{ds32}}{1 + (g_{m32} + g_{mb32})\, r_{ds32}}. \tag{4.13}$$

4.6 Results obtained from NFET-based voltage regulator

This section contains the simulation results of the classical voltage regulator. The pre- and post-irradiation measurements results are also presented and discussed later on.

4.6.1 Simulation results of the NFET-based voltage regulator

Theoretically, the electronic system should be stable if the phase margin equals one degree. However in practice, a margin of 20° – 30° is considered to be a safe value. Extensive considerations about the stability of feedback systems can be found in [76] and [116], and will not be discussed here.

Figure 4.12 shows the Bode diagrams of the presented NFET-based linear voltage regulator. The plots are used to evaluate the phase margin, the unity-gain frequency and the DC gain of the regulator. Usually it is difficult to obtain a high speed system and good stability, while keeping the power consumption at a reasonable level. In the presented regulator the unity-gain frequency is as high as 126.5 MHz with the phase margin of 76°.

[5] r_{ds30} and r_{ds32} are the small-signal drain-to-source resistances of M_{30} and M_{32}, respectively

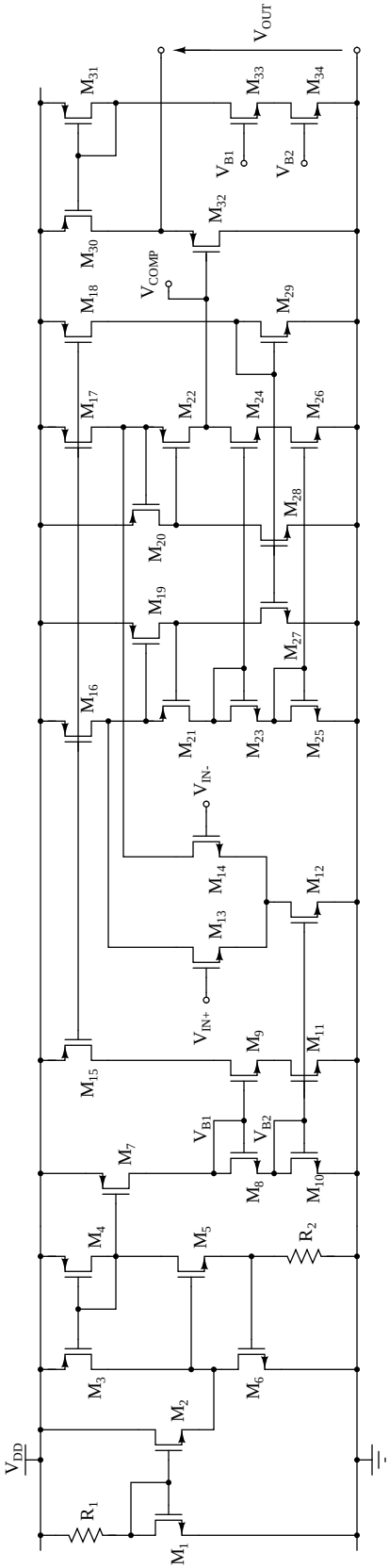

Figure 4.11: Schematic diagram of the error amplifier used in the linear voltage regulator based on the NMOS pass transistor.

Table 4.1: Parameters of the transistors used in the design of the error amplifier shown in Fig. 4.11.

Transistor	Width	Length
M_1	20.0 µm	2.00 µm
M_2	20.0 µm	0.50 µm
M_3, M_4	10.0 µm	5.00 µm
M_5	20.0 µm	0.50 µm
M_6	20.0 µm	2.00 µm
M_7	20.0 µm	5.00 µm
M_8, M_9, M_{10}, M_{11}	2.00 µm	0.50 µm
M_{12}	10.0 µm	0.50 µm
M_{13}, M_{14}	150 µm	0.20 µm
M_{15}	2.00 µm	0.50 µm
M_{16}, M_{17}	12.0 µm	0.50 µm
M_{18}	1.00 µm	0.50 µm
M_{19}, M_{20}	6.00 µm	0.35 µm
M_{21}, M_{22}	10.0 µm	0.15 µm
M_{23}, M_{24}, M_{25}, M_{26}	8.00 µm	0.50 µm
M_{27}, M_{28}	1.50 µm	3.00 µm
M_{29}	3.00 µm	3.00 µm
M_{30}	90.0 µm	0.20 µm
M_{31}	10.0 µm	0.20 µm
M_{32}	50.0 µm	0.14 µm
M_{33}, M_{34}	2.00 µm	0.50 µm

The simulated quiescent current (I_Q) is 380 µA, including 38 µA drawn by the bandgap circuit. For the supply voltage of 1.5 V it gives 570 µW, which is approximately 0.7 % of the total output power.

The DC gain in the feedback loop of the regulator is not required to be very high. In the presented design it is as high as 56.7 dB.

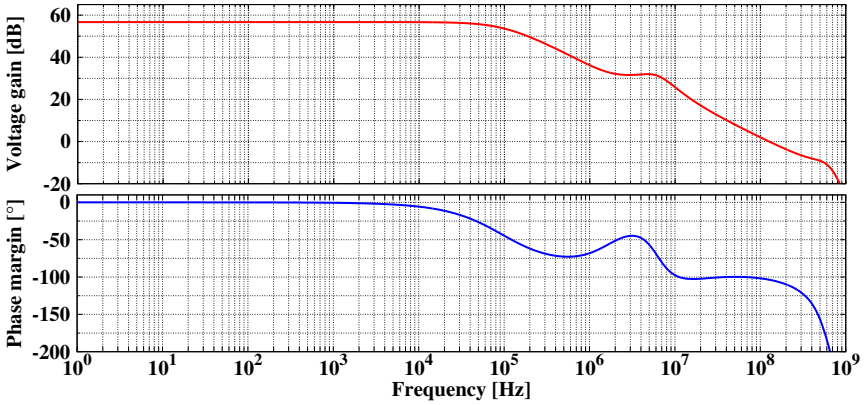

Figure 4.12: Bode plots simulated for the NFET-based voltage regulator, representing the gain and the phase margin as a function of frequency.

The value of the PSRR as a function of frequency is presented in Fig. 4.13. The analogue front-end requires the PSRR of the voltage regulator to be as high as possible. It is especially important in the frequency range between 1 MHz and 10 MHz, where the front-end electronics is the most sensitive to disturbances occurring on the supply line. Therefore, following discussions with the front-end designer it has been decided that the minimum value of the PSRR should be at least 20 dB. In the case of the presented voltage regulator, the lowest PSRR is 17.9dB, observed at a frequency of 2 MHz. At low frequencies it is as high as 73.1 dB.

Transient simulations performed with the Spectre Circuit Simulator (Fig. 4.14) show the time evolution of the voltage in three important nodes of the circuit: the supply line (top), the output of the bandgap circuit (middle) and the output of the voltage regulator (bottom). The supply voltage is ramped up to 1.5 V in 1 ms and V_{REF} and V_{OUT} follow this. It is important to mention that the bandgap circuitry requires a reset signal for proper startup. This signal is applied at 1.1 ms and results in temporary increase (up to 1.46 V) of the reference voltage which then drops down to its nominal value of 637 mV.

In order to simulate the possible voltage fluctuations occurring on the supply line, a periodic voltage step of $V_{p-p} = 50$ mV is applied. The change of the supply voltage triggers small fluctuations of the output voltage, $\Delta V_{OUT} = 133.1$ µV. Hence, the line regulation parameter according to Eq. 4.1 is calculated to be 0.27 %. Figure 4.15 shows

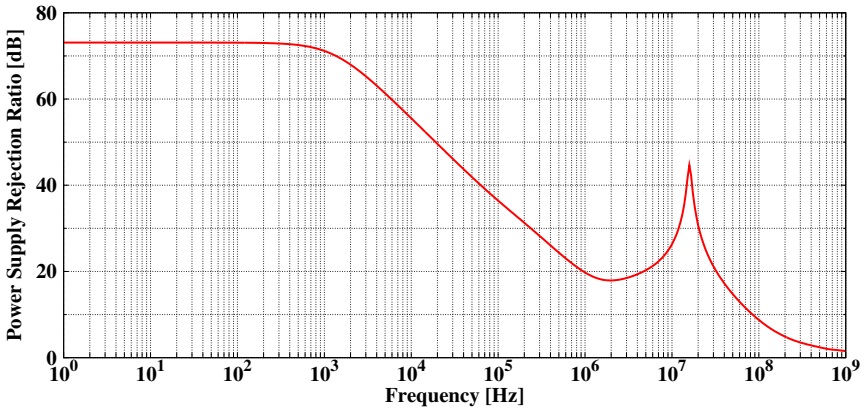

Figure 4.13: PSRR as a function of frequency simulated for the NFET-based voltage regulator.

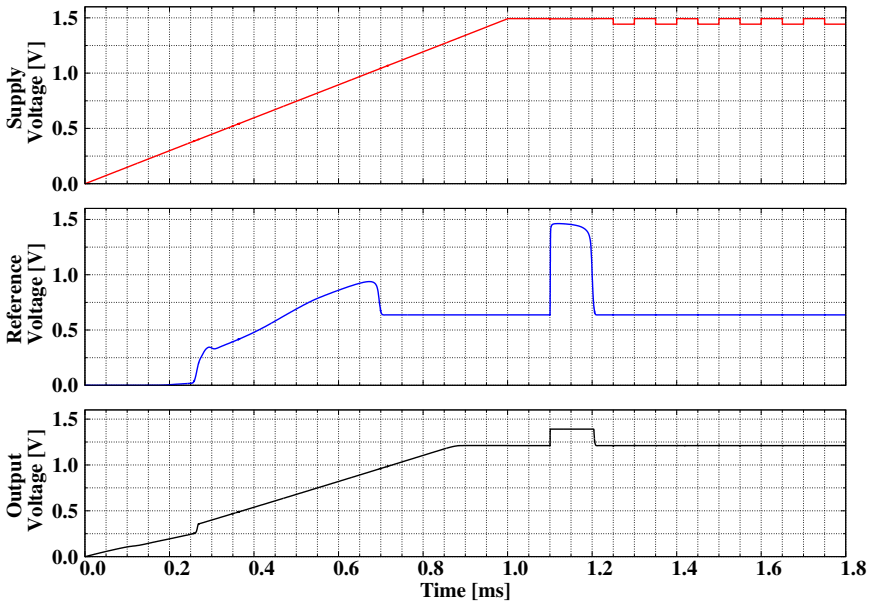

Figure 4.14: The supply voltage (top), the reference voltage (middle) and the voltage response from the proposed classical NFET-based voltage regulator (bottom).

the rising and falling edge of the voltage signal applied at the input of the regulator and the simulated transient response of the circuit.

Another key parameter, the load regulation, is simulated by applying a current step at the output of the regulator. The transient response of a circuit to the current step of 15 mA (around 20 % of the nominal output current value) is shown in Fig. 4.16. The difference between the output voltage levels before and after the current change is applied, is as high as 15.6 µV. The load regulation calculated according to Eq. 4.2 is about 0.1 %. The

transient response simulated for the same current step is $\Delta V_{TR} \approx 7.74\,\text{mV}$.

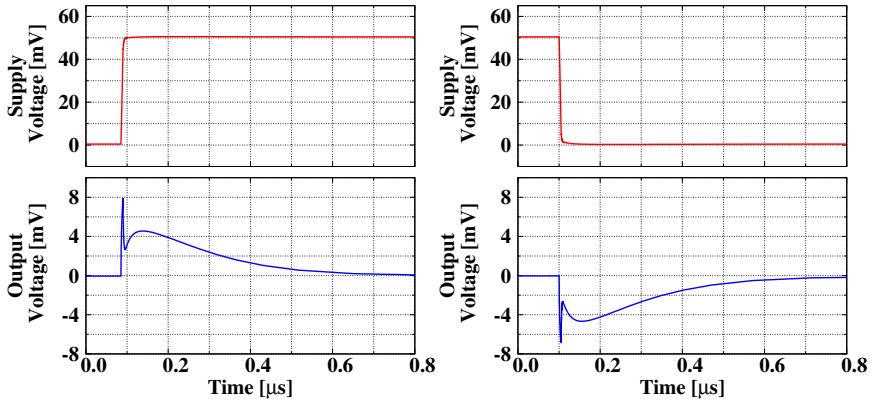

Figure 4.15: The voltage step applied at the output of the NFET-based voltage regulator (top) and the voltage response observed at the output of the circuit (bottom).

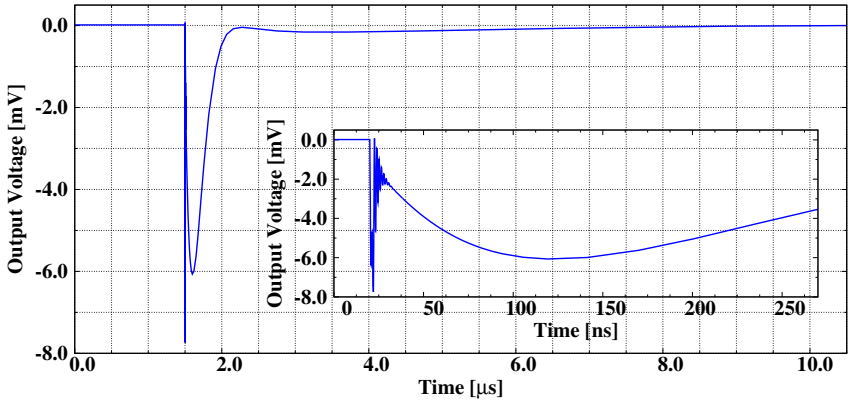

Figure 4.16: Simulated transient response of the NFET-based voltage regulator to the current step of 15 mA applied at the circuitry output.

4.6.2 Test results of the NFET-based voltage regulator

The following paragraphs comprise a discussion of test results from the prototype of the linear voltage regulator employing a zero-V_{th} NMOS pass transistor. To facilitate the comparison of the pre-irradiation and post-irradiation behaviour of the circuit, all the results have been presented in the same section.

The irradiation tests have been performed using the same CERN in-house X-ray generator as previously described in Section 2.3. The prototype chips with the voltage

regulators were mounted on the PCBs (Fig. 4.17), irradiated up to the TID of 200 Mrad within around 60 hours and then annealed at 100 °C for 168 hours.

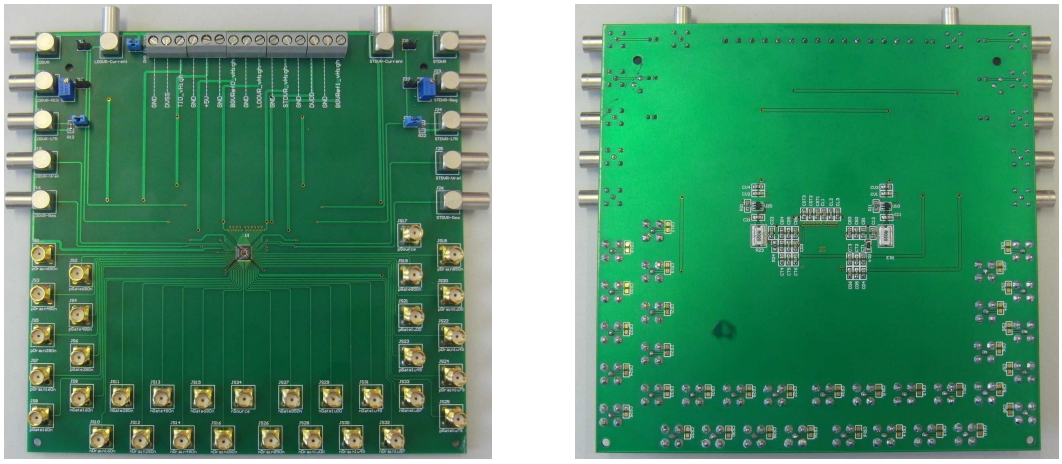

Figure 4.17: The PCB with the prototype chip mounted in the middle.

In order to evaluate the performance of the voltage regulator and its possible application in the future ABCN-13 read-out chip, the following tests have been performed:

- the measurement of the DC transfer characteristics of the voltage regulators;
- the measurement of the DC output characteristics; and
- the measurement of the transient response to a current step applied at the output of the circuit.

The very first measurements have shown that the output voltage from all tested regulators is systematically lower by about 80 mV in comparison with expected 1.2 V. This discrepancy is caused by the low reference voltage provided by the bandgap circuit integrated in the chip. In this case, instead of the simulated $V_{REF} = 637$ mV, a reference voltage of 593 mV has been measured on the chip. In order to investigate this unexpected behaviour some additional simulations of the bandgap circuit were performed. It was discovered that the bandgap circuitry is very sensitive to any current drawn from its output. In particular, a DC current of 600 nA results in the $V_{REF} = 593$ mV, so the same as measured during the tests.

In addition, it has been measured that the value of the reference voltage is not only lower than expected, but also increases monotonically with the TID. The measured percentage change between the initial and post-irradiation (at 200 Mrad) value of V_{REF} is 6 %. It is obvious that the low reference will increase the power losses due to a higher voltage drop on the pass transistor. Despite that fact, the initial (pre-irradiation) value of the power efficiency measured for V_{DD} of 1.5 V is above 74 % and rises up to 78 % at

high TID. The evolution of the measured value of the reference voltage and the power efficiency together with the TID is presented in Fig. 4.18.

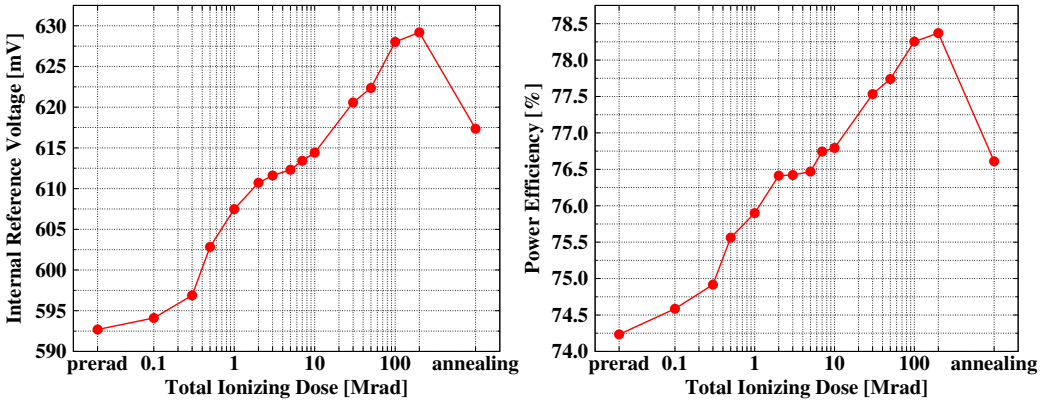

Figure 4.18: Evolution of the reference voltage (left) and the power efficiency (right) of the classical voltage regulator with the TID measured for the supply voltage of 1.5 V.

Figure 4.19 shows the transfer characteristics measured for the presented voltage regulator in two different configurations of the test setup: with an external and internal reference voltage provided by the power supply unit and the integrated bandgap circuit, respectively. In order to measure the transfer characteristics, the input voltage was swept from 1.2 V to 1.6 V and the output voltage was monitored. This procedure has been applied to the pre-irradiated chip and then repeated after every irradiation step, and the annealing. During the test, the regulator was loaded with 70 mA. Figure 4.19 presents five transfer characteristics, measured before the irradiation, for the TID of 1 Mrad, 10 Mrad, 200 Mrad, and after annealing.

The shape of the characteristics does not change significantly during the irradiation. The regulator provides a stable output voltage of 1.2 V for an input voltage range between 1.3 V and 1.6 V, the maximum supply voltage at which the thin gate oxide devices may be operated. The dropout voltage, the minimum source-to-drain voltage at which the pass transistor still has the ability to regulate the voltage, is $V_{DO} = 100\,\text{mV}$.

It has already been mentioned that the reference voltage changes with the TID. This has an influence on the value of the output voltage and the shape of the characteristics. Depending on the dose, the output voltage varies between 1.115 V (pre-irradiation measurement) and 1.182 V (at 200 Mrad). After annealing it drops down again to 1.161 V.

The output characteristics are shown in Fig. 4.20. On the basis of these curves one can estimate the DC output resistance of the regulator. The characteristics have been measured by applying different load to the output of the regulator and monitoring the

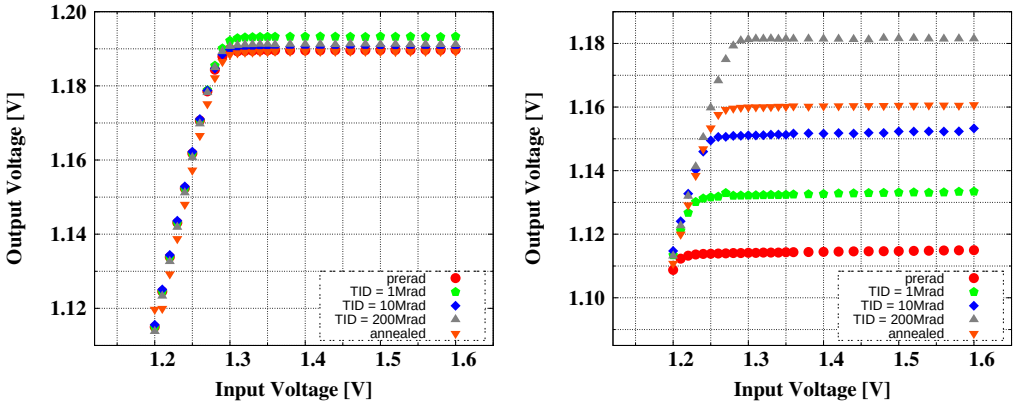

Figure 4.19: Transfer characteristics of the classical voltage regulator measured before the irradiation, for the TID of 1 Mrad, 10 Mrad and 200 Mrad, and after annealing for externally (left) and internally (right) generated reference voltage.

output voltage at the same time. The output current was changed from 40 mA up to 100 mA. The calculated DC output resistance is 0.31 Ω, measured for the circuit with the external reference voltage. The output resistance does not change significantly with the TID. However, it is higher than expected from the simulations. If the internal bandgap circuitry is enabled, R_{OUT} varies between 0.28 Ω and 0.36 Ω

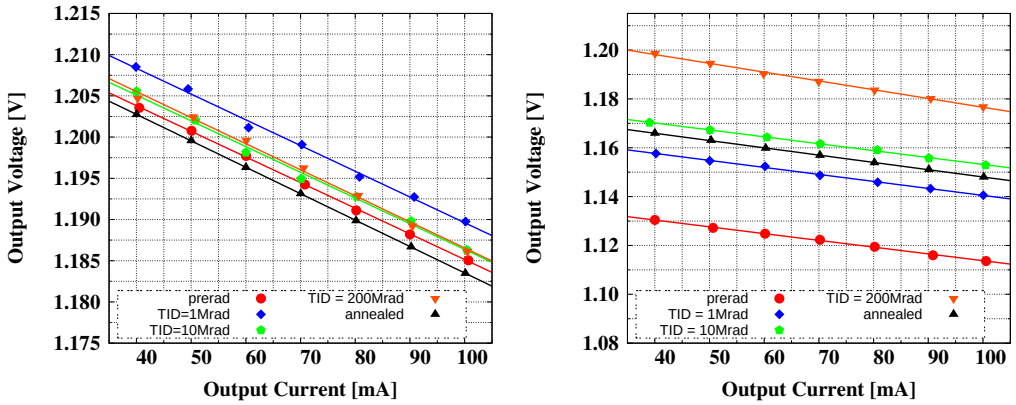

Figure 4.20: Output characteristics of the classical voltage regulator measured before the irradiation, for the TID of 1 Mrad, 10 Mrad and 200 Mrad, and after annealing for externally (left) and internally (right) generated reference voltage.

There are two main sources of the discrepancy observed between the simulation and measurement results. Firstly, the output resistance is intrinsically low so it can be easily increased by the additional parasitic resistance of the bond wires, metal lines on the chip and the PCB, like it was in the case of the switched capacitor DC-DC step-down converter

presented in Chapter 3. Secondly, it has been observed that the Spectre models are not accurate enough and may give incorrect estimates. This issue has already been reported by the FE-I4[6] design team [117].

The transient response to a current step applied at the output of the voltage regulator is presented in Fig. 4.21. In order to obtain these waveforms, the test setup has to be modified by adding a switched resistive load in parallel to the nominal load resistance enforcing the constant output current. The presented results confirm the good AC performance of the regulator. High phase margin allows fast and smooth transient response to be obtained, and no ringing is observed.

It has been measured that a change in the output current of around 14.5 mA causes the output voltage to change by 5.3 mV. The amplitude of the current fluctuation was chosen to correspond to the expected $\pm 20\,\%$ fluctuation of the current consumption in the analogue front-end electronics. The calculated output resistance is slightly above 360 mΩ, similar to the value measured from the output characteristics. The additional 50 mΩ comes from the cabling and the parasitic resistance of the PCB with the switching load. It is worth mentioning that the presented voltage regulator will be integrated on the same silicon die as the analogue front-end electronics, therefore the problem of parasitic resistance will be significantly reduced.

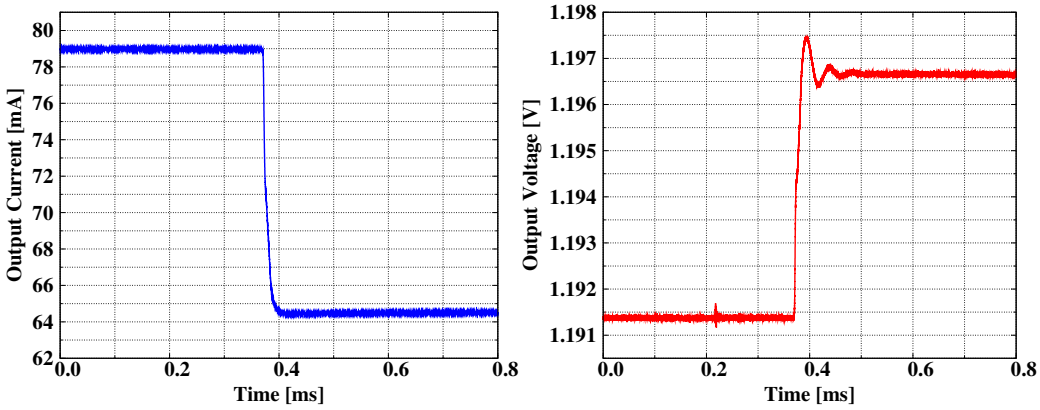

Figure 4.21: Measured transient response of the classical voltage regulator to a current step applied at its output.

[6]FE-I4 is a pixel integrated read-out circuit designed for the ATLAS Inner Detector upgrade.

4.7 Low-dropout regulator using a *p*-channel MOS device for voltage regulation

The second linear voltage regulator prototype presented in this thesis employs a PMOS transistor as a pass element, so it can be called a true LDO voltage regulator. The regulator's output voltage has been set to 1.2 V, compatible with the requirement for the analogue supply voltage of the future ABCN-13 chip. The regulator is equipped with a bandgap voltage reference circuit providing $V_{REF} = 637\,\text{mV}$. However, the reference voltage can also be applied from an external source.

A schematic diagram of the proposed voltage regulator is shown in Fig. 4.22. The entire circuit consists of the following blocks: bandgap voltage reference circuit, *R-C* filter (R_1, R_2, C_1), error amplifier, pass PMOS transistor (M_{PASS}), sensing network (R_{F1}, R_{F2}), compensation network (M_S, C_F, C_C, R_S) and output capacitor C_{OUT}. For simulation purposes the regulator has been equipped with a load resistor R_L. The load capacitor is too big (C_{OUT}=100 nF) to be integrated on a chip, hence an external SMD component must be used. Such a capacitor has a non-zero Equivalent Series Resistance (ESR) which is very important from the viewpoint of the circuit stability and will be discussed later.

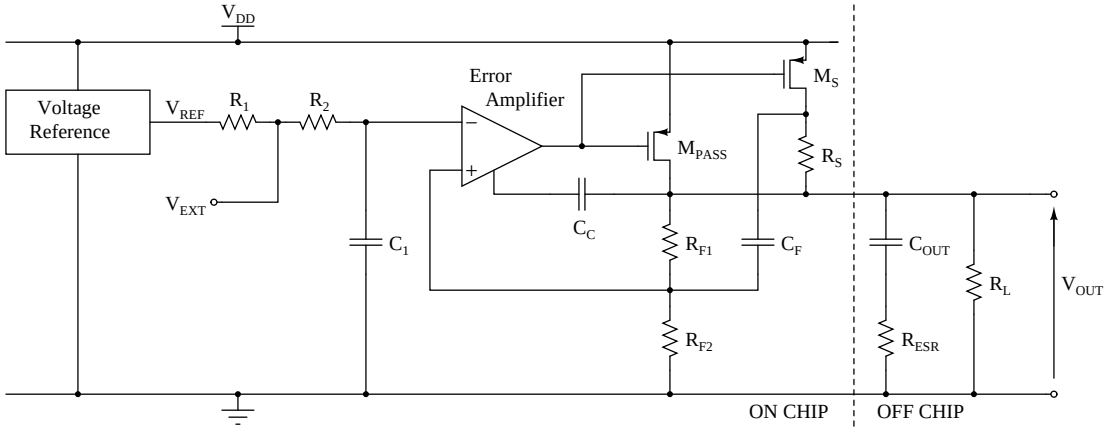

Figure 4.22: Schematic diagram of the linear voltage regulator prototype based on a *p*-channel pass transistor.

The bangap circuit is the same as was used in the previously presented classical voltage regulator. Also the *R-C* filter and the sensing network consisting of resistors $R_{F1} = 50\,\text{k}\Omega$ and $R_{F2} = 56\,\text{k}\Omega$ are identical.

The W/L ratio of the PMOS pass transistor has been calculated to be $125 \cdot 10^3$, so it can handle the output current of 70 mA and maintain the stability of the system. Hence, setting the channel length to the minimum value of 0.12 µm, gives a width of 15 mm.

In order to provide unconditional stability of the system, a slow-rolloff frequency compensation has to be introduced to the LDO circuit. The compensation network consists of the PMOS transistor M_S ($W_S/L_S = 1.00\,\mu\text{m}/0.16\,\mu\text{m}$), resistor $R_S = 6\,\text{k}\Omega$, feedback capacitor $C_F = 2\,\text{pF}$ and the compensation capacitor $C_C = 1.2\,\text{pF}$. The compensation scheme is based on a rolloff technique, as described in [118]. This technique introduces a dominant half-pole whose magnitude rolls off as the square root of frequency, giving a phase shift of only 45°. A half-pole is realised by alternating poles and zeros with a constant frequency ratio. A detailed analysis of LDO voltage regulator circuitry employing the slow-rolloff technique can be found in [119]. The most important fact is that the presented solution allows the circuit to maintain stability despite the changing values of the ESR in the output capacitor.

4.7.1 Design of the error amplifier

The architecture of the error amplifier used in the presented above LDO voltage regulator is very similar to the one presented in Section 4.5.1. The current reference circuit is identical. Small improvements have been made to the bias of the cascode current source. In order to decrease the output resistance of the second stage, an architecture of a super source follower has been used. The entire schematic diagram is shown in Fig. 4.25 and the transistor sizing, in Table 4.2.

First stage of the error amplifier

The first stage of the error amplifier is presented in Fig. 4.9. To improve the voltage swing at the output of the folded-cascode, the classical cascode current sink was replaced by the high-swing cascode current sink [76]. A modified circuit is presented in Fig. 4.23. Due to that change, the output voltage is reduced by the value of V_{th}, while the transistors M_{24} and M_{26} still remain in saturation. The disadvantage of this method is that it increases the power consumption of the amplifier in order to provide proper biasing (transistors M_{B1} and M_{B2}).

Second stage of the error amplifier

For stability reasons, it is important to keep the pole of the amplifier at high frequencies, beyond the unity-gain bandwidth. The output pole of the amplifier is a product of its output resistance and the load capacitance. The presented amplifier is loaded with the gate capacitance of the large *p*-channel transistor, so it is important to keep the output

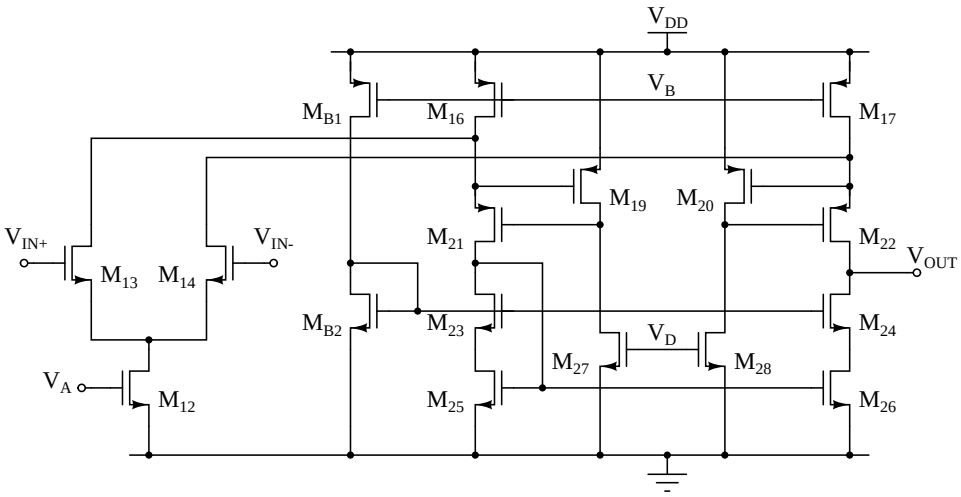

Figure 4.23: Schematic diagram of the first amplifying stage using a high-swing cascode current sink.

resistance at a sufficiently low level. This can be achieved, without the significant increase in the area or power dissipation, by employing the super-source follower architecture [116] shown in Fig. 4.24.

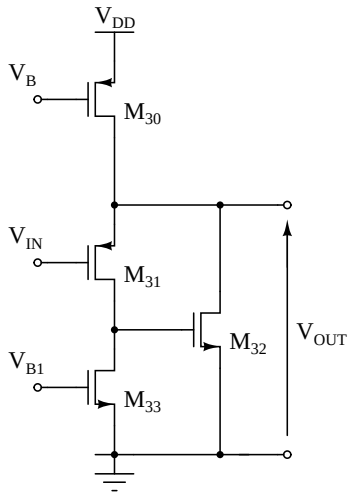

Figure 4.24: Schematic diagram of the super source follower circuit.

The output resistance of the presented circuit is lowered due to the applied negative feedback loop. Assuming that the current sources M_{30} and M_{33} are ideal ($r_{ds30} \rightarrow \infty$ and

$r_{ds33} \to \infty$[7]), the output resistance can be expressed as:

$$R_{OUT} \approx \frac{1}{g_{m31} + g_{mb31}} \left(\frac{1}{g_{m32} \cdot r_{ds31}} \right). \tag{4.14}$$

Comparing equations 4.12 and 4.14, one can immediately note that the output resistance of the super source follower circuit is reduced by a factor of $(g_{m32} \cdot r_{ds31})$ in comparison to the standard source follower architecture.

The voltage gain of the second stage of the error amplifier is also modified by the feedback loop and this is expressed as follows:

$$A_v \approx \frac{g_{m31} \cdot r_{ds31}}{1 + (g_{m31} + g_{mb31}) r_{ds31} + \dfrac{1}{g_{m32} \cdot r_{ds32}}}. \tag{4.15}$$

Therefore, there are two reasons to keep the product $g_{m32} \cdot r_{ds32}$ as large as possible. Firstly, it allows a significant reduction of the output resistance and as a consequence improves the stability of the whole system. Secondly, high $g_{m32} \cdot r_{ds32}$ does not degrade the small-signal voltage gain.

4.8 Results obtained from PFET-based voltage regulator

Due to the fact that the architecture of the LDO voltage regulator presented in this section is similar to the previously discussed classical regulator, all simulations and tests performed to evaluate the circuit are identical. This section contains the results from evaluation and radiation tests for the LDO circuit.

4.8.1 Simulation results of the LDO voltage regulator

An AC analysis (Fig. 4.26) was performed in order to determine the speed and the stability of the LDO regulator. The simulated value of the unity-gain frequency is 60 MHz and the phase margin is close to 70°. The DC voltage gain in the feedback loop is as high as 73.1 dB.

[7] r_{ds30} and r_{ds33} are small-signal drain-to-source resistance of M_{30} and M_{33}

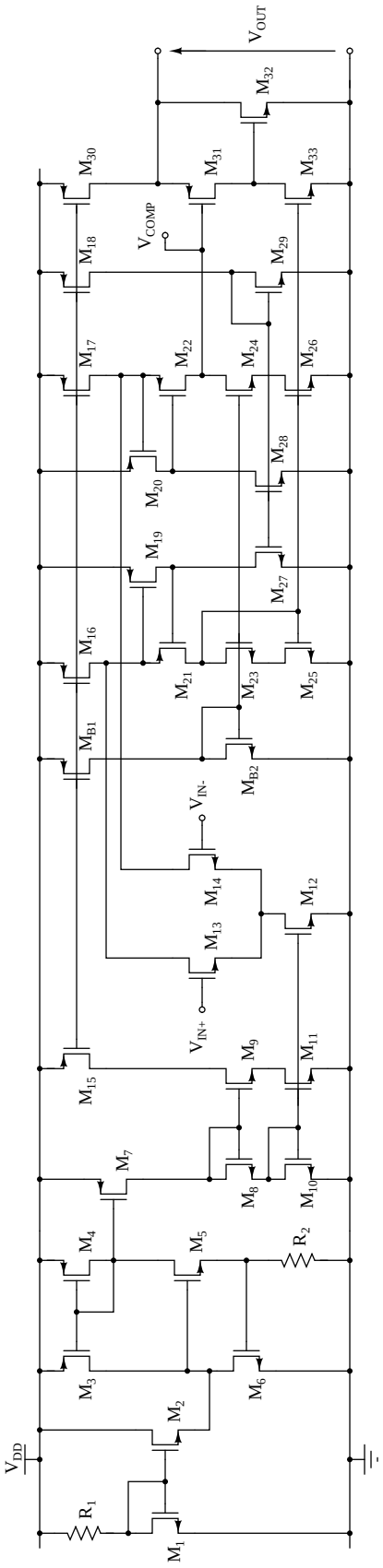

Figure 4.25: Schematic diagram of the error amplifier used in the linear voltage regulator based on the PMOS pass transistor.

Table 4.2: Parameters of the transistors used in the design of the error amplifier shown in Fig. 4.25.

Transistor	Width	Length
M_1	20.0 µm	2.00 µm
M_2	20.0 µm	0.50 µm
M_3, M_4	5.00 µm	5.00 µm
M_5	20.0 µm	0.50 µm
M_6	20.0 µm	2.00 µm
M_7	20.0 µm	5.00 µm
M_8, M_9, M_{10}, M_{11}	2.00 µm	0.50 µm
M_{12}	14.0 µm	0.50 µm
M_{13}, M_{14}	150 µm	0.20 µm
M_{15}	2.00 µm	0.50 µm
M_{B1}	7.00 µm	0.50 µm
M_{B2}	2.00 µm	0.75 µm
M_{16}, M_{17}	15.0 µm	0.50 µm
M_{18}	1.00 µm	0.50 µm
M_{19}, M_{20}	6.00 µm	0.35 µm
M_{21}, M_{22}	10.0 µm	0.15 µm
M_{23}, M_{24}, M_{25}, M_{26}	10.0 µm	0.50 µm
M_{27}, M_{28}	1.50 µm	3.00 µm
M_{29}	3.00 µm	3.00 µm
M_{30}	20.0 µm	0.50 µm
M_{31}	50.0 µm	0.14 µm
M_{32}	50.0 µm	0.15 µm
M_{33}	8.00 µm	0.50 µm

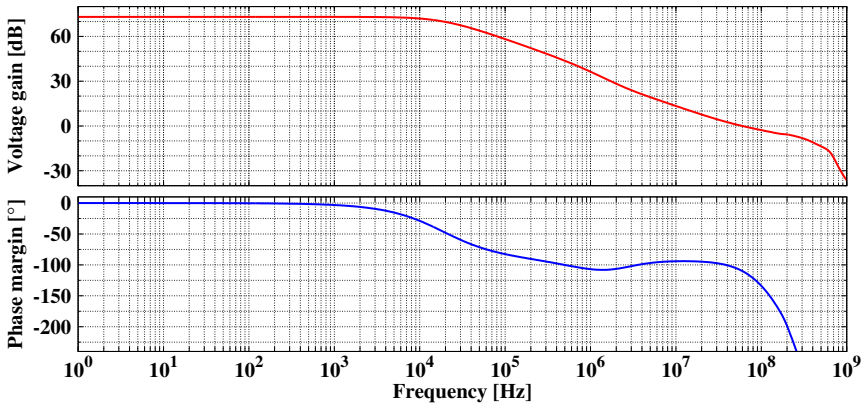

Figure 4.26: Bode plots simulated for the LDO voltage regulator, representing the gain and the phase margin as a function of frequency.

The current consumption for the nominal operation conditions ($I_{OUT} = 70\,\text{mA}$ and $V_{DD} = 1.5\,\text{V}$) is around 500 µA (including 38 µA drawn by the bandgap circuit), which gives the total power of 750 µW. The power consumption is slightly higher than in case of the previous design, because of the biasing circuit used in the high-swing cascode current sink (Fig. 4.9 and Fig. 4.23).

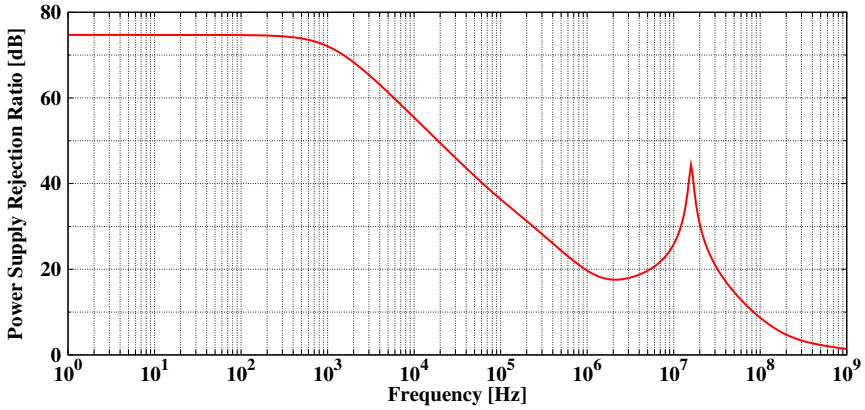

Figure 4.27: PSRR as a function of frequency simulated for the LDO voltage regulator.

The PSRR of the discussed LDO regulator as a function of frequency is presented in Fig. 4.27. At low frequencies its value is determined by the gain of the error amplifier and is as high as 74.7 dB. It drops down for higher frequencies reaching a local minimum of 17.6 dB at 2 MHz.

Figure 4.28 depicts the transient simulation results of the regulator, the supply voltage line (top), the output of the bandgap circuit (middle) and the output of the regulator itself (bottom). A brief description of the simulation procedure can be found in Section 4.6.1.

One can note that the output voltage remains stable despite the fluctuations observed at the supply line. The simulated value of V_{OUT} is 1.21 V.

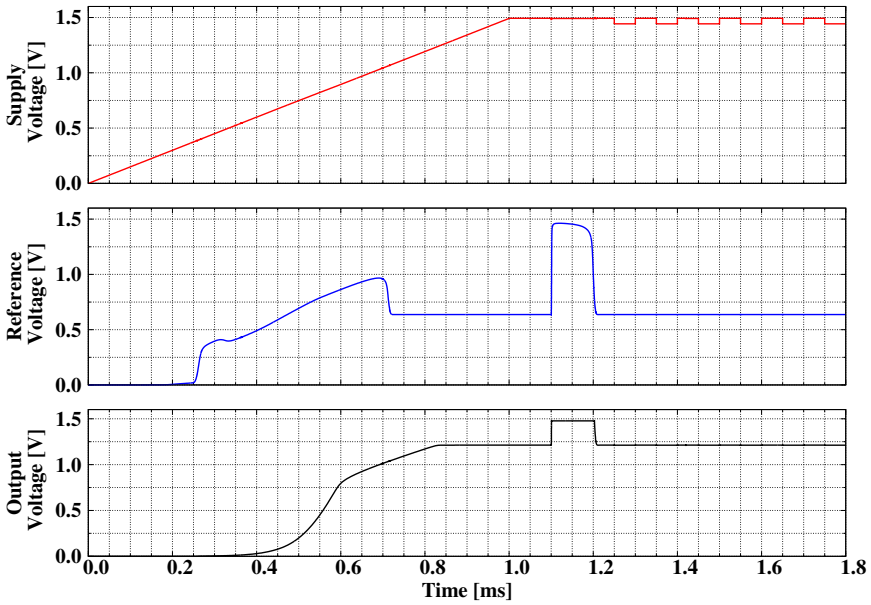

Figure 4.28: The supply voltage (top), the reference voltage (middle) and the voltage response from the proposed LDO voltage regulator (bottom).

The line regulation parameter can be evaluated by applying fluctuations on the supply line and monitoring the output voltage. Hence, voltage pulses with an amplitude of 50 mV result in the output voltage change of 198.1 µV. The rising and falling edges of the voltage step with the transient response of the circuit are shown in Fig. 4.29. According to Eq. 4.1, the calculated line regulation is 0.40 %.

A current step of 15 mA has been applied at the output of the circuit, increasing the load current from 70 mA to 85 mA. The change of the load conditions causes a small shift of the output voltage, $\Delta V_{OUT} = 29.8\,\mu V$. The load regulation calculated as $\Delta V_{OUT}/\Delta I_{OUT}$ is around 0.20 %. The simulated transient response for the current step of 15 mA is $\Delta V_{TR} = 7.33\,mV$. Figure 4.30 shows how the LDO reacts to the output current change.

4.8.2 Test results of the LDO voltage regulator

Both voltage regulator architectures presented in the thesis are similar. The requirements for their operation are identical and so is the measurement procedure. The behaviour of the integrated bandgap voltage reference circuit and the power efficiency of the regulator will not be discussed here, because results obtained are compatible with those presented in Fig. 4.18.

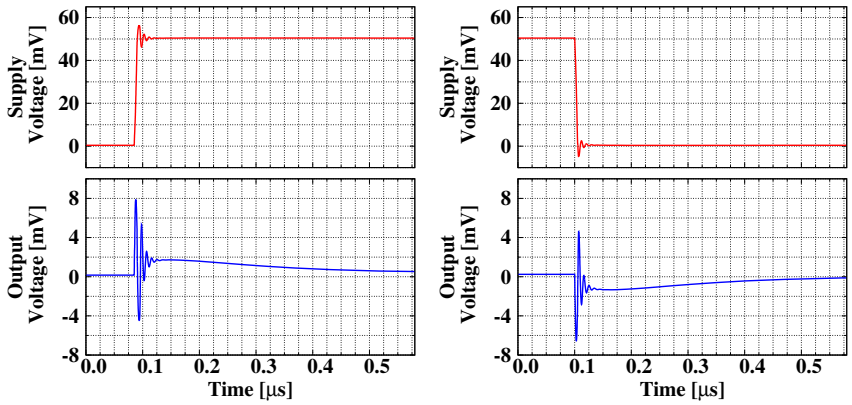

Figure 4.29: The voltage step applied at the output of the of the LDO voltage regulator (top) and the voltage response observed at the output of the circuit (bottom).

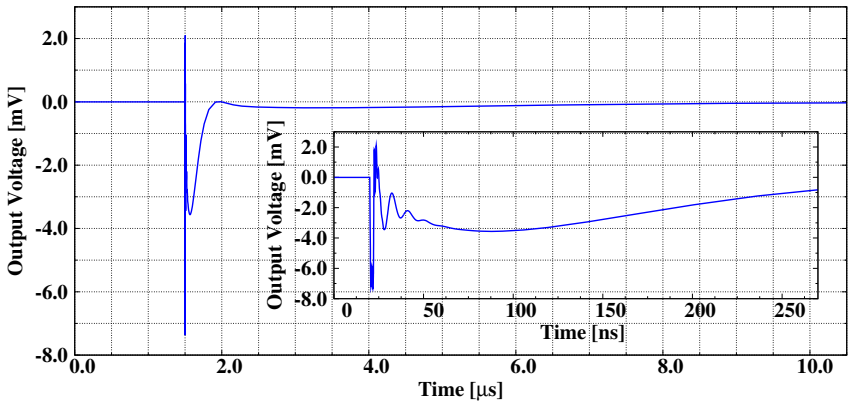

Figure 4.30: Simulated transient response of the LDO voltage regulator to the current step of 15 mA applied at the circuitry output.

Figure 4.31 shows the transfer characteristics measured for the LDO voltage regulator. The presented curves have been measured before irradiation, for the TID of 1 Mrad, 10 Mrad, 200 Mrad and after annealing. They have been collected for the external reference voltage of 637 mV and the internal reference voltage produced by the bandgap circuit. The regulated output voltage for the stable V_{REF} remains close to 1.2 V all the time during the irradiation. The measured dropout voltage is only 50 mV, so half of that of the previously discussed voltage regulator. Due to this fact, the input voltage range is slightly wider, between 1.25 V and 1.6 V. However, if the internal bandgap circuit is enabled the output voltage varies significantly depending on the TID. The initial V_{REF} results in an output voltage of 1.12 V which then rises up to 1.18 V, measured at 200 Mrad.

All the output characteristics presented in Fig. 4.32 have been measured for the supply

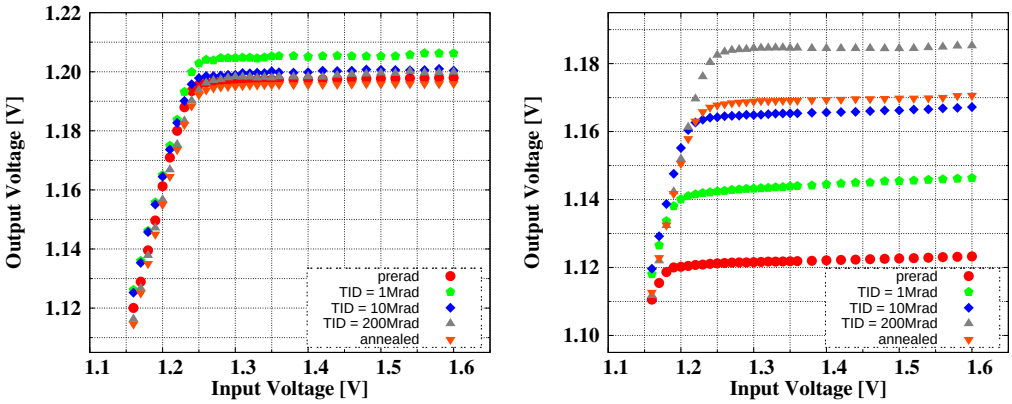

Figure 4.31: Transfer characteristics of the LDO voltage regulator measured before the irradiation, for the TID of 1 Mrad, 10 Mrad and 200 Mrad, and after annealing for externally (left) and internally (right) generated reference voltage.

voltage of 1.5 V and the reference voltage produced either by an external source or the integrated bandgap circuit. The output resistance calculated on the basis of these curves is 0.31 Ω and it remains constant regardless of the TID. There is also no significant difference between the R_{OUT} measured for the external and internal V_{REF}.

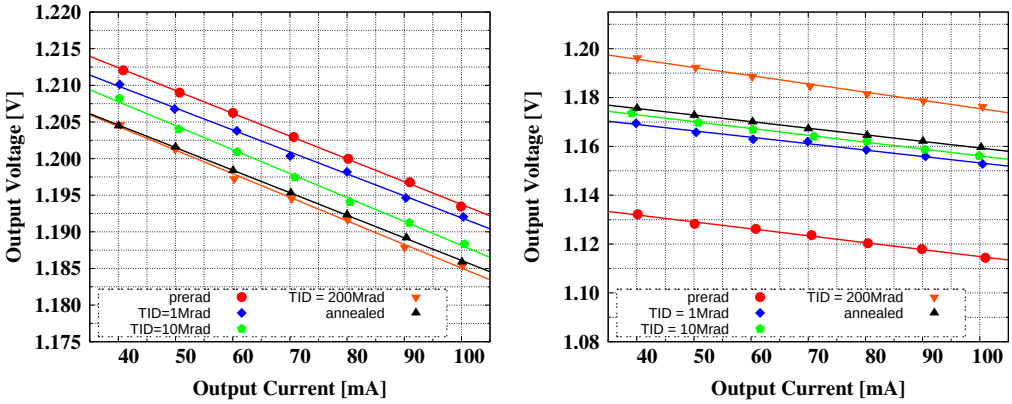

Figure 4.32: Output characteristics of the LDO voltage regulator measured before the irradiation, for the TID of 1 Mrad, 10 Mrad and 200 Mrad, and after annealing for externally (left) and internally (right) generated reference voltage.

The transient response of the LDO to a current step applied at its output is presented in Fig. 4.33. By using a simple switched current source, a step of the amplitude of $\Delta I_{OUT} \approx 14.5\,\text{mA}$ is applied. The output voltage fluctuation caused by the change of the load is $\Delta V_{OUT} \approx 5.4\,\text{mV}$. The output resistance calculated on this basis is around 370 mΩ. However, as has already been mentioned, it will further be reduced if the regulator is

integrated in the same chip as the read-out electronics.

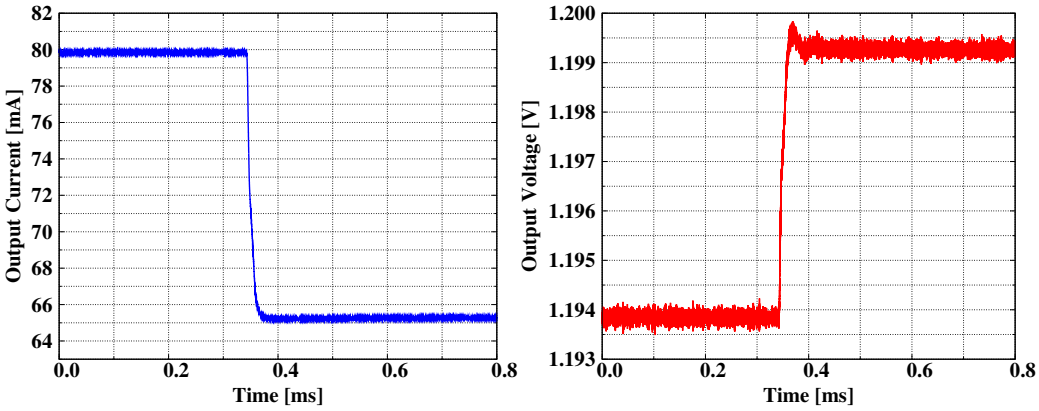

Figure 4.33: Measured transient response of the LDO voltage regulator to a current step applied at its output.

4.9 Design of the VREG013 chip

The VREG013 chip is a $2 \times 2\,\mathrm{mm}^2$ ASIC designed and manufactured using the IBM 130 nm CMOS technology. The layout of the chip from the Cadence Virtuoso Layout Editor™ and its microphotograph are presented in Fig. 4.34a and 4.34b, respectively. The chip contains two prototypes of the linear voltage regulators, planned to be used in the design of the future ABCN-13 chip.

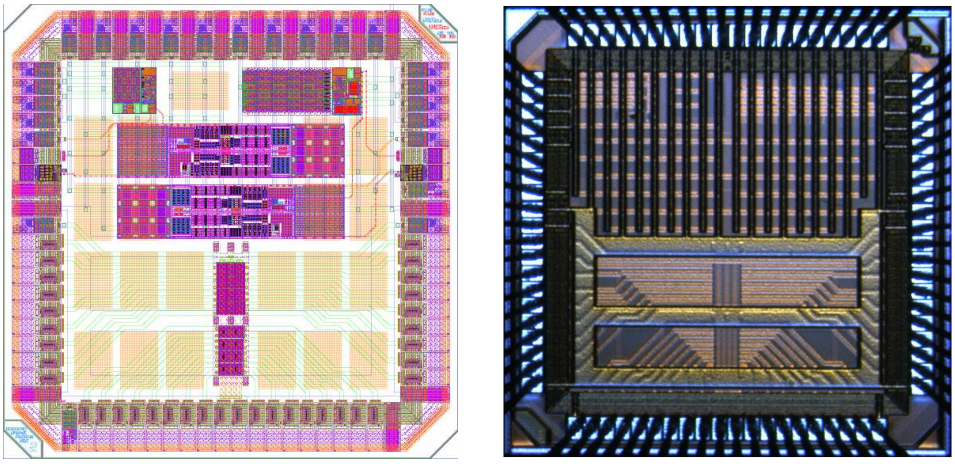

Figure 4.34: Layout of the DCDC013 from Cadence Virtuoso Layout Suite (left) and the microphotograph of the chip bonded to a PCB (right).

Each voltage regulator, the classical one based on the zero-V_{th} n-channel transistor and the PMOS-based LDO, are additionally equipped with separate bandgap voltage reference

circuits with dimensions of $1000 \times 200\,\mu m^2$. The chip is also equipped with two arrays of complementary transistors (NFETs and PFETs), designed for irradiation tests of CMOS structures at low temperatures. The transistors making up these arrays are identical to the devices used in the digital standard cells.

Similarly to the DCDC013 chip, the VREG013 is also equipped with 80 short pads provided by the IBM library. Only 36 pads are used by the voltage regulators. The remaining 44 are used by the transistors in the TID matrices. The multiple power and ground pads are interleaved in order to reduce possible power losses and wire bond inductances. Each voltage regulator is supplied with a separate power domain but the ground is common. Also each bandgap circuit has a dedicated power pad. Although the bandgap circuit is meant to provide a constant voltage of 637 mV, there are dedicated pads allowing an external V_{REF} if needed. The same pads allow the value of the reference voltage to be monitored.

4.9.1 Layout of the NFET-based voltage regulator

The layout of the linear voltage regulator, using a zero-V_{th} *n*-channel transistor is shown in Fig. 4.35. The design is compact and occupies an area of around $0.1\,mm^2$ ($520 \times 200\,\mu m^2$). Around 75 % of the silicon area is occupied by the pass transistor. The remaining 25 % of area is used by the error amplifier, sensing and compensation network, *R-C* filter, and substrate connections (guard-rings).

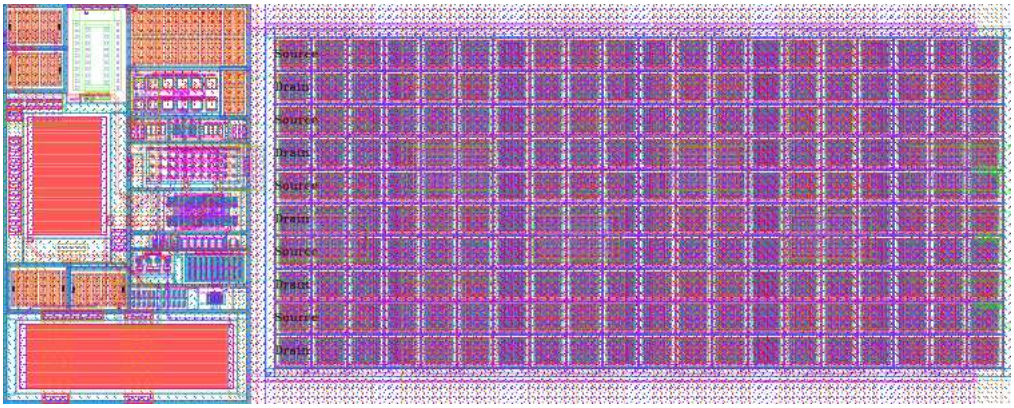

Figure 4.35: Layout of the linear voltage regulator employing a zero-V_{th} NMOS transistor as a pass device.

The voltage regulator is also equipped with a bandgap voltage reference circuit. Its dimensions are $1\,mm \times 0.24\,mm$. Therefore, the total area of the voltage regulator, including this bandgap reference is $0.34\,mm^2$.

4.9.2 Layout of the PFET-based voltage regulator

The layout of the prototype LDO linear voltage regulator is shown in Fig. 4.36. It comprises of all the blocks (*R-C* filter, error amplifier, compensation and sensing network), apart from the bandgap voltage reference circuitry and the load capacitor which is meant to be external.

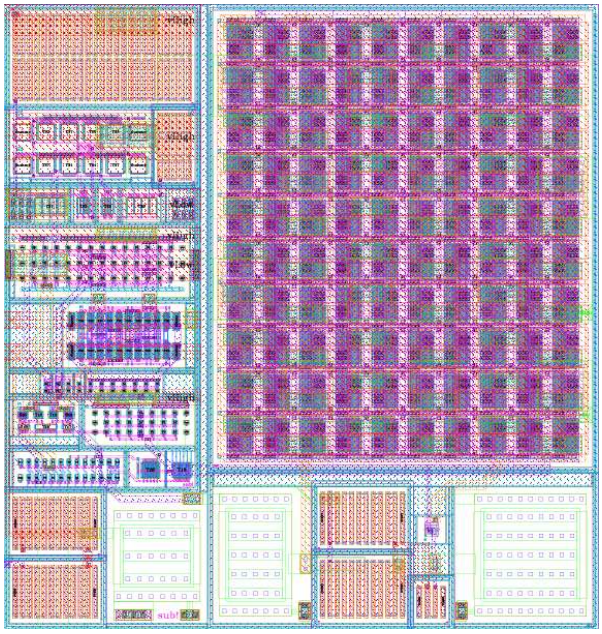

Figure 4.36: Layout of the linear voltage regulator employing a *p*-channel transistor as a pass device.

The presented design of the LDO voltage regulator is very compact, with total area less than 0.04 mm^2. A major part, around 50 %, of the total silicon area is occupied by the large PMOS pass transistor. The error amplifier (16 %), the the compensation and sensing network (25 %) and and the contact to the bulk (9 %) comprise the remaining 50 %.

4.10 Conclusions on the VREG013 development

This chapter presents two prototypes of the linear voltage regulators, the classical design based on the *n*-channel MOS transistor and the LDO circuit employing the *p*-channel transistor as a pass device. Both circuits have been integrated on the VREG013 chip manufactured in the IBM 130 nm CMOS process.

The presented voltage regulators provide a stable and clean supply voltage of 1.2 V which can be used to supply the analogue front-end electronics on the future ABCN-13

chip. Both architectures, one employing a zero-V_{th} *n*-channel transistor in the classical source follower configuration and the other, a *p*-channel transistor in the common source configuration, allow a very low dropout voltage of 100 mV and 50 mV to be obtained, respectively.th This translates to a significant increase in the power efficiency of the regulators. The irradiation tests of the VRAG013 chip do not exhibit any noticeable performance degradation of the regulators, if a stable external reference voltage is applied.

However, there are two issues which have been discovered during the tests of the prototype chip. Firstly, the reference voltage provided by the integrated bandgap circuit is too low and it varies with the TID. The measured value of V_{REF} is 40 mV lower than expected and changes by 6 % during the irradiation. This problem will be solved by replacing the existing bandgap circuit by a block which is more radiation tolerant. Secondly, the measured output resistance is higher than expected from simulations and this affects the performance of the regulators by increasing the load regulation parameter. A major part of this resistance comes from the parasitic elements on the PCB and will not be an issue when the regulators are integrated on the same chip as the analogue read-out electronics. It is also possible that the models used in the simulations have some limitations and do not allow for correct estimation of the output resistance. Thus, some further studies of the power distribution on the layout and modelling are needed.

Summary

The development of the new powering scheme for the front-end electronics is a key aspect of the future ATLAS detector upgrade because is affects directly the performance and research potential of the upgraded detector. Extensive studies in this field have been ongoing for the last few years. This dissertation presents designs of four integrated circuits, which are foreseen to be used in the considered powering schemes. The developed circuits are: switched capacitor DC-DC step-up and step-down converters, and two linear voltage regulators, a classical architecture using an NMOS transistor and an LDO employing a PFET as a pass device. The step-up converter and one of the voltage regulators are planned to be used in the serial powering scheme, while the step-down converter has been designed to be implemented in the parallel powering scheme.

All discussed circuits have been designed and manufactured in the IBM 130 nm CMOS process. Their required specification is to a large degree dictated by the specific environment expected in the future detector, thus the presented circuits must be characterised by a very high power efficiency and good radiation tolerance. In order to meet these requirements the design phase must be preceded by a careful analysis of the power budget in each of the proposed circuits. Good radiation tolerance of the design can be achieved by employing special design techniques.

The radiation tolerance is a crucial issue, so the behaviour of the various types of transistors must be well understood. The future read-out chip will operate in a very high radiation field. Thus, it was necessary to perform the irradiation tests of the semiconductor structures manufactured in the technologies which are the main candidates for the electronics upgrade. The dedicated test structures have been irradiated and tested at room temperature, and their intrinsic radiation tolerance has been compared. It has been proven that radiation resistance of the IBM 130 nm CMOS is adequate to meet the requirements for the front-end electronics upgrade. Further irradiation tests at low temperature are scheduled for the near future. The conclusions presented in Chapter 2 have been taken into account in the designs presented later in this dissertation.

The design of the switched capacitor DC-DC converters presented in Chapter 3

has been driven by the power efficiency. Both discussed circuits are planned to be integrated on the future ABCN-13 read-out chip. Special emphasis has been put on the reduction of power losses occurring in the switching MOSFETs. Thus, the converters are characterised with very high power efficiencies, 85 % and 91 % for the step-up and step-down converter, respectively. As a result the output voltages obtained from the power converters are very close to the values required by the design specification. The impact of the parasitic inductance of the bond wires on the performance has also been taken into account. The use of interleaved pads and triple-well transistors allowed for a significant reduction of switching noise observed at the output. The poor quality of the output voltage can be further improved by applying one of the methods proposed by the author in the conclusions to that chapter. The post-irradiation degradation of the converters' performance is clearly visible, but fully acceptable. Further improvement of radiation tolerance can be obtained by implementing enclosed gate geometry layout of the large switches. It is worth mentioning that the next generation of the step-down converter is under development and will be used in the design of the second version of the CBC readout chip for the CMS tracker upgrade [106]. This would be a good opportunity to verify the converters' behaviour on a fully bump bonded chip.

The linear voltage regulators discussed in Chapter 4 are the last stages of the powering chain in the serial powering scheme. Both designs are able to provide a stable and clean voltage supply for the analogue electronics on the ABCN-13 chip. In the thesis two different architectures have been presented. During the prototype testing the correct functionality of both the voltage regulators has been shown. They fulfill the requirements concerning the level of the output voltage, output current range and voltage regulation. Both architectures allow for very low values of the dropout voltage which result in significant reduction of power losses and high power efficiency. Although the overall performance of the voltage regulators is good, the behaviour of the bandgap circuit has been found to be a serious limitation. The low value of the reference voltage is a result of poor current drive capability of the bandgap circuit. This issue can be fixed by adjusting the resistor values in the sensing network. During the irradiation tests, it was discovered that the reference voltage changes with the Total Ionizing Dose causing output voltage fluctuations. It has been concluded that in order to provide required output voltage the bandgap circuit must be improved or replaced by a design with better radiation tolerance.

In the context of the ATLAS Inner Detector upgrade project many challenges present themselves for the development of the new front-end ASIC powering scheme. The work presented here demonstrated that it is possible to implement high performance on-chip power converters and linear voltage regulators compatible with demanding requirements

of high power efficiency, good radiation tolerance and minimal additional external components. These building blocks create a foundation upon which future powering systems in the ATLAS experiment will be built.

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